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Approved by A.I.C.T.E.

Fundamentals of Electronics Engineering

Course Level: Undergraduate

Credit: 3

Prepared by:

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Course Content:

Module-I: Basics of semiconductor (6L)

Conductors, Insulators, and Semiconductors- crystal structure, Fermi Dirac function, Fermi level, Energy band diagrams, valence band, conduction band, and band gap; intrinsic, and extrinsic (p-type and n-type) semiconductors, position of Fermi level in intrinsic and extrinsic semiconductor, drift and diffusion current – expression only (no derivation) , mass action law , charge neutrality in semiconductor, Einstein relationship in semiconductor , Numerical problems.

P-N Junction Diode and its applications (3L)

p-n junction formation and depletion region, energy band diagram of p-n junction at equilibrium and barrier energy, built in potential at p-n junction, energy band diagram and current through p-n junction at forward and reverse bias, Static and Dynamic resistance of Diode, Transition capacitance and diffusion capacitance-I characteristics and current expression of diode, temperature dependencies of V-I characteristics of diode, p-n junction breakdown – conditions, avalanche and Zener breakdown, Concept of Junction capacitance, Zener diode and characteristics.

Diode half wave and full wave rectifiers (centre tapped and bridge) circuits and operation ($I_{DC,}$ I_{rms}, $V_{Dc,}V_{rms)}$, ripple factor without filter, efficiency, PIV, TUF; Reduction of ac ripples using filter circuit (Qualitative analysis); Design of diode clipper and clamper circuit - explanation with example, application of Zener diode in regulator circuit. Numerical problems.

Module-II: Bipolar junction transistor (BJT) (6L)

Concept of "Transistor", Formation of PNP/NPN Transistors, energy band diagram, current conduction mechanism, CE, CB, CC configurations, transistor static characteristics in CE, CB and CC mode, junction biasing condition for active, saturation and cut-off modes, current gain α, β and γ, early effect.

Biasing and bias stability; biasing circuits - fixed bias; voltage divider bias; collector to base bias, D.C. load line and Quiescent point, calculation of stability factors for different biasing circuits.

BJT as an amplifier and as a switch – Graphical analysis; Numerical Problems.

Field effect transistor (FET) (3L)

Concept of "field effect", Classification of FETs-JFET, MOSFET, operating principle of JFET. Drain and transfer characteristics of JFET (n-channel and p-channel), CS, CG, CD configurations, Relation between JFET parameters. FET as an amplifier and as a switch– graphical analysis. E-MOSFET (n-channel and p-channel),D-MOSFET (n-channel and p-channel), Numerical Problems.

Module-III: Feedback and Operational Amplifier (8L)

Concept of feedback with block diagram, positive and negative feedback, gain with feedback. Feedback topologies, effect of feedback on input and output impedance, distortion, concept of oscillation and Barkhausen criterion.

Operational amplifier – electrical equivalent circuit, ideal characteristics, non-ideal characteristics of op-amp – offset voltages; bias current; offset current; Slew rate; CMRR and bandwidth, Configuration of inverting and non-inverting amplifier using Op-amp, closed loop voltage gain of inverting and non-inverting amplifier, Concept of virtual ground, Applications op-amp – summing amplifier; differential amplifier; voltage follower; basic differentiator and integrator, Numerical Problems.

Module-IV: Digital Electronics (8L)

Digital Electronic Principles

Introduction, Binary digits, Logic levels and Digital waveforms, Introduction to basic logic operation, Number system, Decimal numbers, Binary numbers, Decimal-to-Binary conversion, Simple binary arithmetic.

Logic Gates and Boolean Algebra

The inverter, The AND, OR, NAND, NOR, Exclusive-OR and Exclusive-NOR gate, Boolean operations and expressions, Laws and Rules of Boolean algebra, DeMorgan's theorem, Boolean analysis of logic circuits, Standard forms of Boolean expressions, Boolean expression and truth table.

Module-V: Communication System, Satellite and Radar System and Wireless communication (8L)

Principles of Communication: Fundamentals of AM & FM, Transmitters & Receivers, Satellite and Radar System and Wireless communication

Project Domains:

1. Zener diode in voltage regulation
2. Amplifier design using BJT
3. Amplifier design using FET
4. Circuit design using Op-Amp

Text Books:

1. D. Chattopadhyay, P. C. Rakshit, Electronics Fundamentals and Applications, New Age International
2. Millman&Halkias, Integrated Electronics, Tata McGraw Hill.
3. Boylestead and Nashelsky, Electronic Devices and Circuits Theory, 9/e, PHI, 2006.

Reference Books:

1. Sedra& Smith, Microelectronics Engineering.
2. John D. Ryder, Electronic Fundamentals and Applications, PHI
3. J.B.Gupta, Basic Electronics, S.K. Kataria.
4. Malvino: Electronic Principle.
5. Schilling &Belove: Electronics Circuits

Module-I 6L
Basics of semiconductor

Introduction: In this module we study discrete electronic energy levels in atoms which are spread into energy bands in a crystal. The band structure gives the idea of classifying different types of materials. Regarding the study of the transport phenomena in materials we observe that the current in a metal is due to the flow of negative charges (electrons), whereas the current in a semiconductor results from the movement of both electrons and positive charges (holes). A semiconductor may be doped with impurity atoms so that the current is dominated either by electron or by holes. The transport of the charges in a crystal is due to the influence of an electric filed (a drift current), and due to a no uniform concentration gradient (a diffusion current) is investigated.

1.1 Conductors, Insulators, and Semiconductors

Materials around us can be classified as

i) Conductors,
ii) Semiconductors and
iii) Insulators.

This classification is made based on

i) the conductivity level and
ii) band gap energy of the material.

Classification based on conductivity:

Metal: High conductivity. Example- copper, silver, gold, iron etc. Value of conductivity is more than 10^3 mho/cm.

Insulator: Not conductive at all. Example –glass, rubber, teflon etc. Value of conductivity is less than 10^{-7} mho/cm.

Semiconductor: Conductivity level is in between metal and insulator. Value of conductivity is 10^{-7} to 10^3 mho/cm.

The difference between the energy level between conduction band (uppermost filled band) and valence band (lowermost filled band) is known as forbidden energy gap (E_G).

Classification based on band gap energy:

Meta: Gap is nil i.e. conduction band and valence band overlaps.

Semiconductor: This gap is about 1eV.For germanium and silicon, forbidden energy gap is 0.78 eV and 1.2 eV respectively at 0 K.

Insulator:It is more than semiconductor .For example for diamond it is 6 eV.

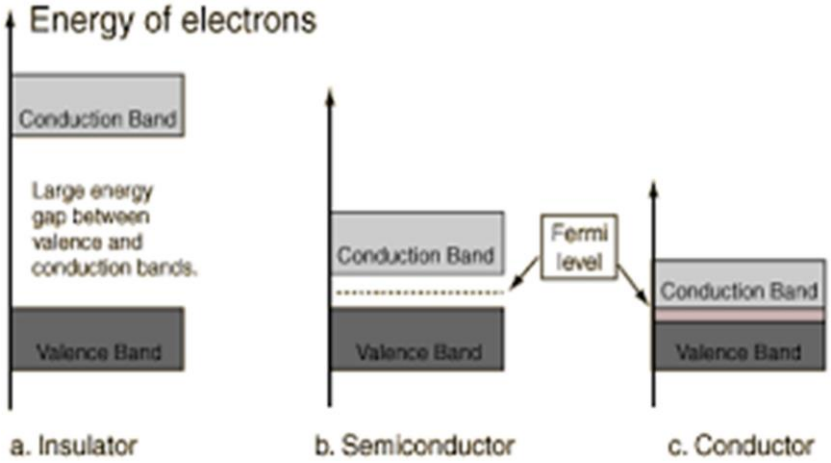


Fig 1.1 Fig showing band gap of different materials

1.2 Crystal Structure

A crystal is a solid consisting of regular and repetitive arrangement of atoms or molecules in space. X- ray and other studies reveal that most metals and semiconductors are crystalline in nature. A crystal consists of space array of atoms or molecules in 3-dimensional regular repetitive structure. The positions of the atoms in the crystal are depicted by points, known as lattice points and we get a crystal lattice.

1.3 Fermi-Dirac Function

The concept of Fermi-Dirac (FD) distribution function is used to give the probability of occupancy of a given state by an electron. The distribution function expression is as follows

$f(E) = 1/1+\exp[(E-E_F) / KT]$

Where f (E) = the probability of occupancy of a given state with energy E,

E_F =the energy of Fermi level,

T = the absolute temperature and

K = Boltzmann constant =1.38 x 10^{-23} J/K

Fermi level

When E=E_F, from equation (1) we get f (E) = ½ for T> 0.Thus the Fermi level is the energy level for which the probability of occupancy is 1/2 for a finite non-zero temperature.

1.4 Energy band diagrams

Valence band, conduction band, and band gap

There are large number of atoms in the crystalline structure of a semiconductor. The total energy (sum of kinetic and potential) is negative and has discrete values. These discrete energy levels can be represented by horizontal lines. Every single atom has a energy line. This large number of discrete and closely spaced energy levels form an energy band. We observe two types of energy band. The lowest energy bands are normally completely filled by the electrons since the electrons always tend to occupy the lowest available energy bands .This energy band is known as **valence band**. The higher energy band may be completely empty or may be partly filled known as **conduction band**. The difference in the energy level between conduction band and the valence band is known as forbidden energy gap or simply **band gap (E_G).** Band gap in semiconductor depends upon temperature. At room

Temperature	Semiconductors	Band gap
Room temperature (300K)	Germanium (Ge)	1.1 eV
	Silicon (Si)	0.72 eV

Table 1.1 Temperature, band gap of two semiconductors

1.5 Intrinsic, and extrinsic (p-type and n-type) semiconductors

Intrinsic semiconductors: If the electrical conductivity of a semiconductor is entirely determined

By the carriers which are generated by thermal agitations from the valence band to the conduction band, the semiconductor is known as pure or intrinsicsemiconductors. Examples includegermanium and silicon.

In an Intrinsic semiconductors the number of holes is equal to the number of free electrons. Thermal agitation continues to produce new electron- hole pairs, where as other electron- hole pairs disappear as a result of recombination. The hole concentration p must equal the electron concentration n so that

$$n = p = n_i$$

where n_i is called the intrinsic concentration .

1.6 E**xtrinsic (p-type and n-type) semiconductors:**

1.6.1 N-type semiconductors

The salient features of N-type semiconductors are as follows:

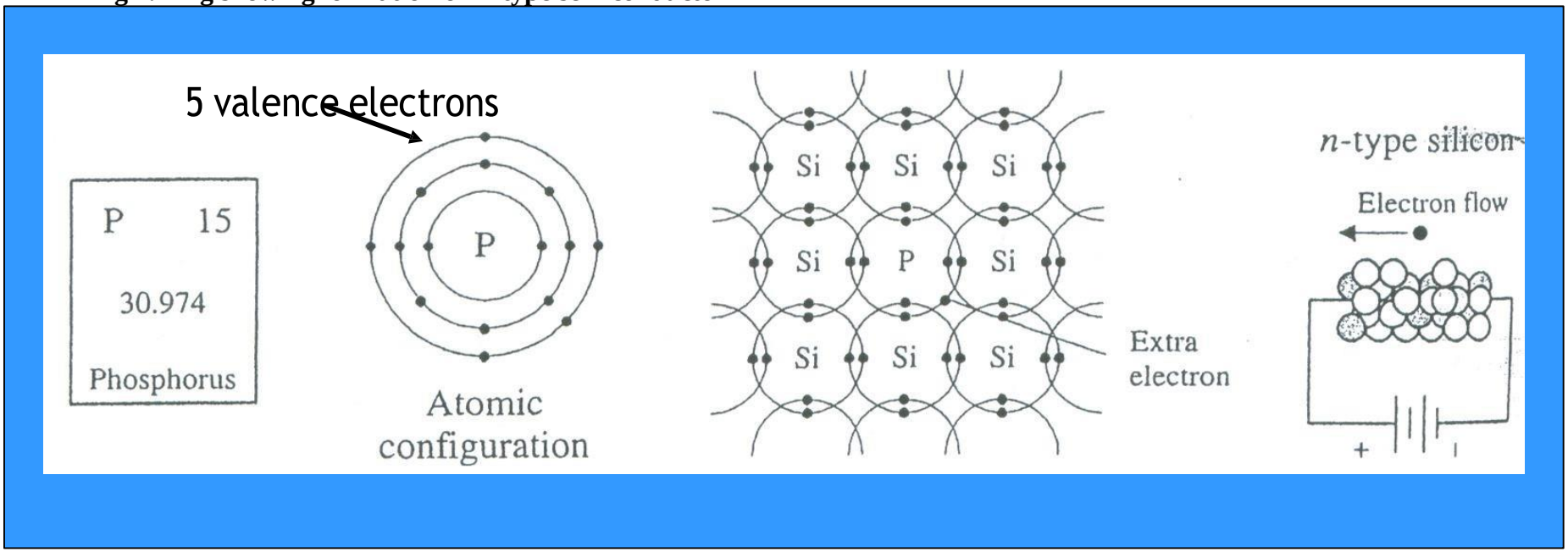
i) N-type semiconductor is formed by doping the elements of Group V (Pentavalent) elements with intrinsic semiconductor like Ge or Si.

ii) Pentavalentimpurities such as phosphorus, arsenic, antimony, and bismuth have 5 valence electronsin the outermost orbit.

iii) For example, when phosphorus impurity is added to Si, every phosphorus atom's four valence electrons are locked up in covalent bond with valence electrons of four neighboring Si atoms. However, the 5^{th} valence electron of phosphorus atom does not find a binding electron and thus remains free. These free electrons behave as the majority carrier of the N-type semiconductor.

iii) The pentavalent impurities are referred to as donor impurities.

Fig 1.2 Fig showing formation of N-type semiconductor



1.6.2 P-Type Semiconductor

The salient features of P-type semiconductors are as follows:

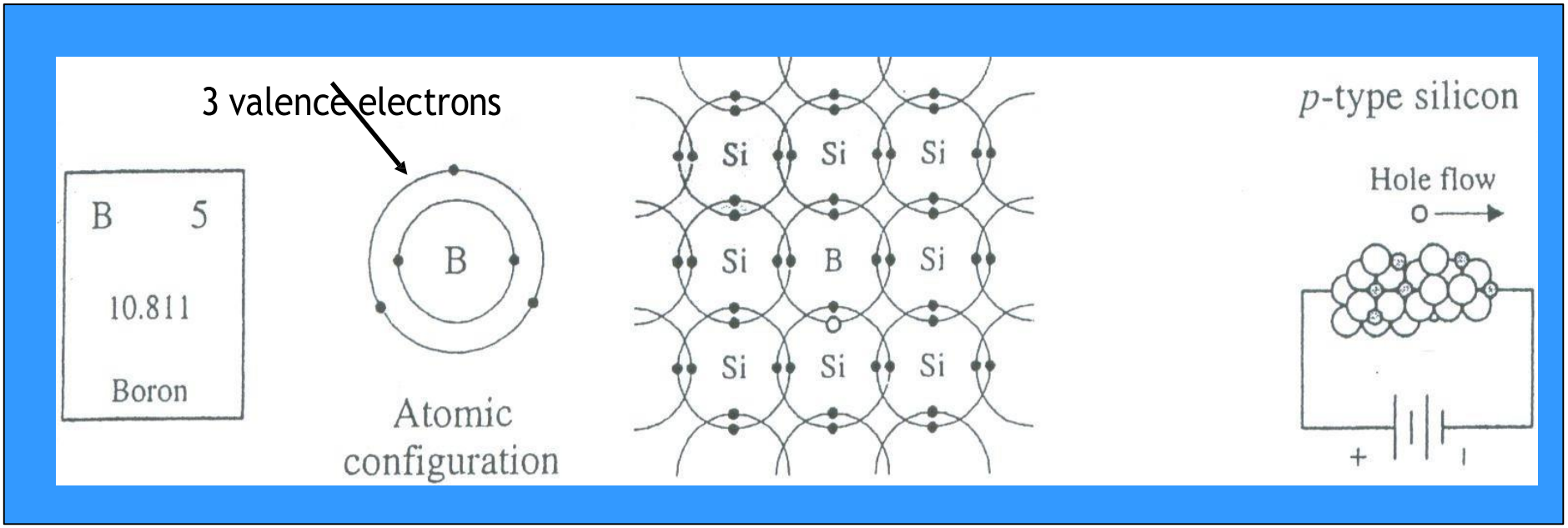
i) P-type semiconductor is formed by doping the elements of Group III (Trivalent) elements with intrinsic semiconductor like Ge or Si.

ii) Trivalent impurities such as boron, aluminum, indium, and gallium have 3 valence electrons in the outermost orbit.

iii) For example, when boron is added to Si, every boron atom's three valence electrons are locked up in covalent bond with valence electrons of three neighboring Si atoms. However, a vacant spot "hole" is created within the covalent bond between one boron atom and a neighboring Si atom. The holes are considered to be positive charge carriers. These holes behave as the majority carrier of the P-type semiconductor.

iv) The trivalent impurities are known as acceptor impurities.

Fig 1.3 Fig showing formation of P-type semiconductor



1.7 Position of Fermi level in intrinsic and extrinsic semiconductor

Intrinsic Semiconductor: The Fermi level lies in the middle of the band gap for an intrinsic semiconductor. This is because, the no of electrons in the conduction band and the no of holes in the valence band are the same.This also implies that the probability of finding an electron near the conduction band edge is same as the probability of finding a hole at the valence band edge.

Extrinsic semiconductor: The Fermi level positions are given below:

N-type semiconductor: Fermi level is nearer to the conduction band of a n-type semiconductor.

For an n-type semiconductor, there are more electrons in the conduction band than there are holes in the valence band. This also implies that the probability of finding an electron near the conduction band edge is larger than the probability of finding a hole at the valence band edge. Therefore, the Fermi level is closer to the conduction band in a n-type semiconductor.

P-type semiconductor: Fermi level is nearer to the valence band of a p-type semiconductor.

For a p-type semiconductor, there are more holes in the valence band than there are electrons in the conduction band. This also implies that the probability of finding an electron near the conduction band edge is smaller than the probability of finding a hole at the valence band edge. Therefore, the Fermi level is closer to the valence band in an n-type semiconductor.

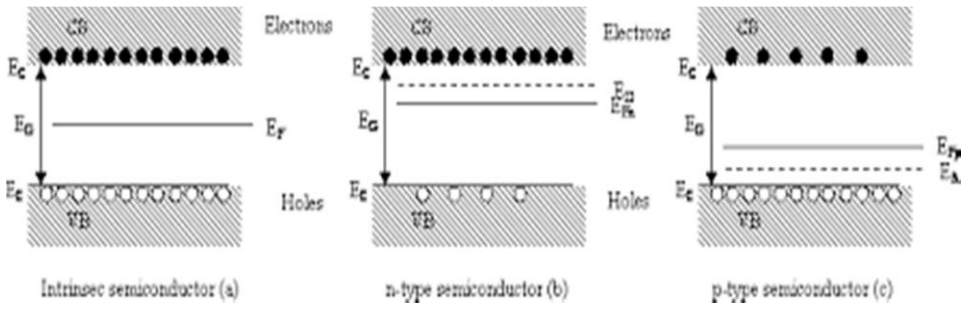


Fig 1.4: Intrinsicsemiconductor N-**typeP-type semiconductor P-type semiconductor**

1.8 Law of Mass Action

In thermal equilibrium the product of electron and hole concentration is always a constant and equal to the square of intrinsic carrier concentration *i.e.*,

$$\square_0 \square_0 = \square_i^2$$

where $\square_0$and$\square_0$are equilibrium electron and hole concentration respectively and $\square_i$ □□ intrinsic carrier concentration,

1.9 Drift Current

The drift current is defined as the flow of electric current due to the motion of the charge carriers under the influence of an external electric field.

Drift current due to the charge carriers such as free electrons and holes are the current passing through a square centimeterperpendicular to the direction of flow.

1.10 Drift Current Density

The total current density due to the drift of both electrons and holes

$$\square_x(\square\square\square\square\square) = (\square_{nx} + \square_{px})_{drift} = (\square\square\square_n + \square\square\square_p)\square_x = \square\square_x$$

where□ - Number of free electrons per cubic centimeter.

□ - Number of holes per cubic centimeter

$\square_n$ – Mobility of electrons in cm^2 / V.s

$\square_p$ – Mobility of holes in cm^2 / V.s

$\square_x$ – Applied Electric filed Intensity in +ve x direction in V /cm

□ – Charge of an electron = 1.6 x 10^{-19} coulomb.

Thus the conductivity due to both types of carriers

$$\square = \square\square\square_n + \square\square\square_p$$

1.11 Diffusion Current

The diffusion of charge carriers is as a result of a gradient of carrier concentration. In this case concentration of charge carriers tends to distribute themselves uniformly throughout the semiconductor crystal. This movement continuous until all the carriers are evenly distributed throughout the material. This type of movement of charge carrier is called diffusion current.

1.12 Diffusion Current Density

Current flows in a semiconductor due to diffusion process in absence of an electric field and the diffusion current density can be obtained by multiplying the particle flux by charge

$$\square_x(\square\square\square\square) = (\square_{nx})_{diff} + (\square_{px})_{diff} = \square\square_n \frac{\square\square}{\square\square} - \square\square_p \frac{\square\square}{\square\square}$$

Where, $\square_n$□□□□$\square_p$ is the diffusion coefficient of electrons and holes.

$\frac{dn}{dx}$□□□$\frac{dp}{dx}$ is the rate of change of electron and hole concentration in +ve x direction.

1.13 Current due to both Drift and Diffusion

In many semiconductors the electrons and holes move by both drift and diffusion in the presence of both the electric field and the carrier concentration gradient. Thus the total electron and hole current density due to drift and diffusion is given by the following expression

$$\square_{nx} = (\square_{nx})_{drift} + (\square_{nx})_{diff.} = \square\square\square_n\square_x + \square\square_n \frac{\square\square(\square}{\square\square)}$$

and $\square_{px} = (\square_{px})_{drift} + (\square_{px})_{diff.} = \square\square\square_p \square_x - \square\square_p \frac{dp(x)}{dx}$

1.14 Einstein Relation

Both the mobility and the diffusion are statistical phenomena. So, $\square$ and $\square$ are not independent. The relationship between them is given by Einstein equation:

$$\frac{\square_p}{\square_p} = \frac{\square_n}{\square_n} = \square_T$$

where $\square_T$ is the volt equivalent of temperature and is defined as

$$\square_T = \frac{\square_B \square}{\square}$$

where, $\square_B$ is the Boltzmann's constant in joules per kelvin and $\square$ is the charge associated with each charge carrier. $\square$ is the temperature in degree Kelvin.

1.15 Equation of Continuity

The equation of continuity states that the net rate of increase in the number of charge carriers in any volume of a semiconductor is the difference of net increase due to flux and generation (thermal or other processes) of carriers and net decrease due to loss by recombination process.

The continuity equation for holes can be represented as,

$$\frac{\&\square}{\&\square} = -\frac{\&\varphi_p}{\&\square} + \square_p - r_p \square$$

Where $\square_p$ is the generation rate of holes and φ_p is the hole particle flux. $\frac{p}{c_p}$ is the recombination rate and r_p is the lifetime of holes.

Similarly, continuity equation for electrons can be expressed as,

$$\frac{\&\square}{\&\square} = -\frac{\&\varphi_n}{\&\square} + \square_n - r_n \square$$

Where φ_n is the electron particle flux, $\square_n$ is the generation rate of electrons. $\frac{n}{c_n}$ is the

recombination rate and r_n is the lifetime of electrons.

Solved Examples

Example 1. Calculate the probability that an energy level $2KT$ above the Fermi level is occupied by an electron at $T = 300$ K.

Solution: The probability of occupation of an energy level by electron is given by Fermi Dirac distribution function as

$$\square(\square) = \frac{1}{1 + \square\square\square\left(\frac{E-E_f}{KT}\right)} = \frac{1}{1 + \square\square\square^{\frac{2KT}{KT}}} = \frac{1}{1 + \square\square\square 2}$$

$= 0.1192 = 11.92\ \%$.

Example 2. Find out the intrinsic resistivity of Ge at 300 K if the intrinsic carrier concentration of Ge at 300 K be $2.33 \times 10^{19}\ \square^{-3}$. ($\square_n = 0.39\ \square^2/\square.\ \square$ and $\square_p = 0.19\ \square^2/\square.\ \square$)

Solution: Intrinsic conductivity of Ge is

$$\square_i = \square\square_i(\square_n + \square_p)$$

$$= 1.6 \times 10^{-19} \times 2.33 \times 10^{-19}(0.39 + 0.19) = 216\ \square/\square.$$

Intrinsic resistivity, $\square_i = \frac{1}{\sigma_i} = \frac{1}{2.16} = 0.46\ fi.\ \square.$

Example 3. (a) Calculate the percentage increase of conductivity of pure silicon at 300 K if it be doped p-type with boron concentration of $5 \times 10^{17}\ \square^{-3}$. ($\square_i = 1.5 \times 10^{16}\ \square^{-3}$, $\square_n = 0.15\ \square^2/\square.\ \square$, $\square_p = 0.045\ \square^2/\square.\ \square$)

(b) Also calculate the electron and hole concentration of n-type silicon if its resistivity be $0.01\ fi.\ \square$.

Solution: (a) Intrinsic conductivity of silicon is

$$\square_i = \square\square_i(\square_n + \square_p) = 1.6 \times 10^{-19} \times 1.5 \times 10^{16} \times 0.195 = 0.468 \times 10^{-3}\ \text{S}$$

When doped with boron, conductivity becomes

$$\square_p = \square\square\square_p = \square\square_A\square_p \qquad (\square \approx \square_A)$$

$$= 1.6 \times 10^{-19} \times 5 \times 10^{17} \times 0.045 = 3.6 \times 10^{-3}\ \text{S}$$

Percentage increase of conductivity = $\frac{3.6-0.468}{3.6} \times 100 = 86.94\%$

(b) Here $\sigma_i = 0.01 fi.\ \square$ and $\square = \square\square\square_n$ $= \frac{1}{\rho} = 10^2 \square/\square$

$$= 10^2 = 1.6 \times 10^{-19} \times \square \times 0.15$$

$$\square = 4.166 \times 10^{21} m^{-3}$$

From the law of mass action $n_0 p_0 = n_i^2$

$$p_0 = \frac{n_i^2}{n_0} = \frac{(1.5 \times 10^{16})^2}{4.166 \times 10^{21}} = 5.4 \times 10^{10} cm^{-3}$$

Example 4. Consider a semiconductor doped with a donor density N_D and no acceptors. Let $n_i = 10^{10}/cm^3$ for the semiconductor.Determine the free electron and hole densities in equilibrium if N_D is $10^{12}/cm^3$ b)$10^{18}/cm^3$

Solution: From Mass action law $n.p = n_i^2$

and also $N_D + p = N_A + n$ (Since the semiconductor is electrically neutral, the magnitude of the positive charge density must equal that of negative charge density).

Given $N_A = 0$. (no acceptors)

So,$N_D + n_i^2/n = n$ which implies $n^2 - n.N_D - n_i^2 = 0$.

$N = [N_D + \sqrt{(N_D + 4n_i^2)}]/2$.

Substituting forn_i^2 and $N_D$we get,

a) For $N_D = 10^{12}/cm^3$,$n = 1.0001 \times 10^{12}/cm^3$ $p = 9.999 \times 10^7/cm^3$
b) For $N_D = 10^{18}/cm^3$, $n = 10^{18}/cm^3$: $p = 10^2/cm^3$

Choose the correct alternative

1 Which of the following element does not have five valence electrons?
a) Phosphorous b) Arsenic
c) Antimony d) Indium

2 The following atoms can act as donors in Si
a) Phosphorous b) Arsenic
c) Gallium d) Indium

3 The Fermi level of an n-type semiconductor lies

a) Near the conduction band edge b) near the valence band edge
c) at the middle of the forbidden gap d) none of the above

4. Diffusivity and mobility are related by
(a) Continuity equation (b) Poison's equation
(c) Einstein's equation (d) Gauss Law

5. Equation of continuity in a semiconductor signifies

(a) Conversion of energy of mobile charge carriers

(b) Conversion of momentum of mobile charge carrier

(c) Conversion of charge of mobile charge carriers

(d) Conversion of charge of ionized donors and acceptors

6. The magnitude of thermal energy *(□□)* at 300 K is

(a) 1.2 eV (b) 0.8 eV (c) 0.25 eV (d) 0.026 eV

Write answer to the questions

1 Differentiate between p-type and N-type semiconductors.

2 Name the doping materials used for their formation.

3 Why silicon is mostly preferred as a semiconductor material.

4 Compare metal, semiconductor, insulator with respect to conductivity, band gap energy , position of Fermi level

5 Define lattice point, Fermi level, Intrinsic concentration of semiconductor,acceptor,donor

6. Give a physical interpretation of Einstein's equation.

7. State the law of mass action in a semiconductor.

8. Give a physical interpretation of Continuity equation.

9. Define mobility and diffusivity. What are their units in SI system?

Solve the problems

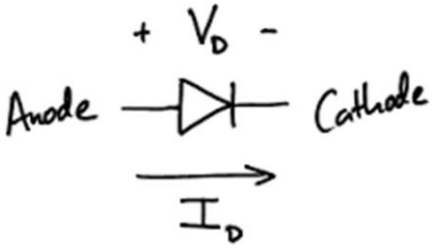
1 At 300K the intrinsic carrier concentration of silicon is 1.5×10^{16} /cm^3.If the electron and hole mobilities are 0.13 and 0.05 m^2 / (V.s) respectively, determine the intrinsic resistivity of silicon at 300 K. (Ans 2315 ohm.meter)

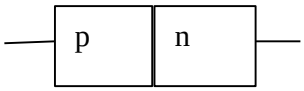
2 Find the concentration of donor atoms to be added to an intrinsic Ge sample to produce an n-type material of conductivity 480 S/m. the electron mobility in n-type Ge is 0.38 m^2 /(V.s) (Ans 7.9×10^{21} /m^3)

MODULE 1
PART 2: PN JUNCTION DIODE AND ITS APPLICATIONS 8L

Introduction:

1. A two terminal semiconductor pn junction based electronic component with the terminals connected to the p and n sides termed the anode and cathode.
2. Its basic function is to allow current flow in one direction and not in the reverse. Under a special circumstance it allows current flow in the reverse direction.
3. Its circuit description is the relationship between the current through vs the voltage across the diode which is nonlinear.
4. The general circuit symbol and structure of diode are shown in the figure.





5. Diodes in electronics are used in ac to dc conversion (as a rectifier), light emission, source of reference voltage, sunlight to electric energy conversion, light detection, etcetera.

Review of Semiconductor:

1. It is a material whose conductivity (the ease with which charge can flow through the material) is between a conductor and an insulator. Its conductivity can be controlled by addition of small amounts of extra material in a process called doping.
2. There are two types of charge carriers: positive holes in the valence band and negative electrons in the conduction band.In a p type the majority charge carrier is the hole and in n type the majority charge carrier is the electron.
3. There are two current mechanisms: drift current which is charge flow due to the force applied by an electric field; diffusion current which is charge flow due to a combination of concentration gradient and random thermal motion.
4. The basic or intrinsic semiconductor can be elemental (silicon) or compound (gallium arsenide).

PN Junction formation and depletion region:

1. When a p type semiconductor is brought into contact with a n type semiconductor a pn junction results.
2. There are three modes of operation: no bias in which no external potential difference is applied across the junction, forward bias in which the anode is at a higher potential than the cathode and reverse bias in which the cathode is at a higher potential than the anode.
3. Here it is assumed that the basic semiconductor is silicon with a valence 4 and the p type acceptor atom is A with a valence 3 and the n type donor atom is D with a valence 5.

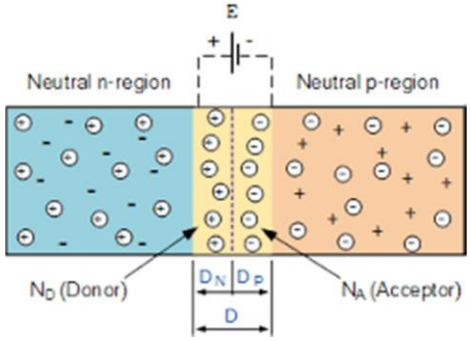
4. In the p type, an acceptor atom (A) in place of a silicon atom will most likely attract an electron from a neighboring silicon atom to complete its covalent bond leaving behind a hole in the silicon atom and become ionized.Thus $A^3 = A^{-4} + h^+$.
5. In the n type, a donor atom (D) in place of a silicon atom will most likely donate an electron to the crystal and complete its covalent bond and become ionized. Thus $D^5 = D^{+4} + e^-$.
6. Each ionized dopant atom with its associated charge carrier forms a neutral system.

No Bias:

1. When the p and n type are brought into contact, initially diffusion currents flow across the physical junction; holes from p to n and electrons from n to p.
2. The hole entering the n material will most likely combine with an electron near the junction annihilating both (meaning the free electron reenters the covalent bond) exposing the D^{+4}ion: $D^{+4} + e^- + h^+ = D^{+4}$.
3. The electronentering the p material will most likely combine with a hole near the junction annihilating both (with the same meaning) exposing the ion A^{-4}ion: $A^{-4} + h^+ + e^- = A^{-4}$.
4. The net result is that an electric field builds up across the junction from the D^{+4} ions to the A^{-4} ions. The field is in such a direction as to push the hole back to the p type and pull the electron back to the n type, that is, a build up of a drift process opposing the diffusion process.

Built-in potential in pn junction:

5. When equilibrium is reached, a strong field exists across the junction such that the drift balances the diffusion and no net junction current flows. The junction field results in a junction potential (potential difference = electric field x distance).
6. The region on both sides of the junction in which the field exists is called the **depletion region** since it is devoid of charge carriers. The width depends on the doping level; higher the doping, smaller the width since more ions are exposed over a smaller region.



Forward Bias:

1. When an external potential difference is applied across the pn junction, the external field is in such a direction as to reduce the internal junction field so that the drift component is reduced which results in the diffusion current reflowing across the junction.
2. In the n/p type the hole/electron entering from the p/n type combines with an electron/hole but now the lost electron/hole is replaced from the external circuit and a continuous current flows through the junction whose conventional direction is from anode to cathode. The current increases exponentially with bias.
3. The energy level diagram is shown below for the case of no bias and forward bias. The +y axis is electron energy (-y axis is hole energy) and the x axis is distance across diode.The energy reference is the vacuum level, that is, the energy required to transport the electron from within the semiconductor to without. The Fermi energy shows typical electron energy level in a material. In n type, it is close to the conduction band energy and in p type it is close to the valence band energy. If there is energy difference across a region, then since force = the negative rate of change of potential energy (F = -dV(x)/dx), there is a force acting on the electrons to move them from higher to lower energy region.In a pn junction, when initially formed, the average electron energy of the p region will thus rise since electrons are added to the material, the average electron energy of the n region will thus fall since holes are added to the material, till the Fermi energies of p, n regions equalize. This is why the p energy levels are higher than n energy levels in a pn junction. The energy difference equals electron charge x junction potential. Under forward bias, the bias field lowers the electron energy difference by an amount electron charge x bias potential.

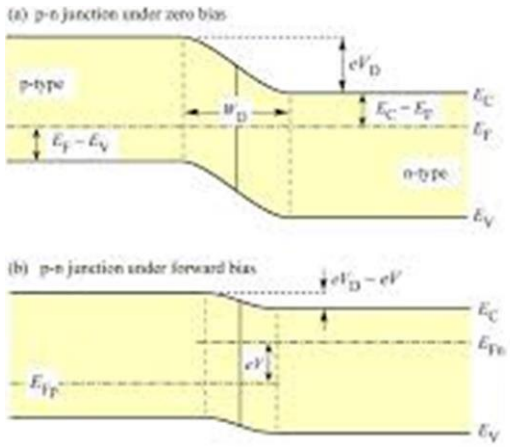


Fig. 4.1. P-n junction under (a) zero bias and (b) forward bias. Under forward bias conditions, minority carriers diffuse into the neutral regions where they recombine.

Fig :Energy band diagram of pn junction

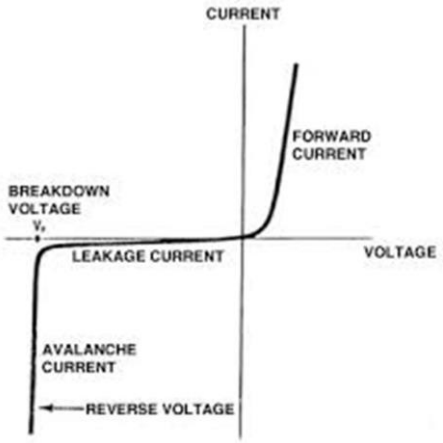
Reverse Bias:

1. When an external potential difference is applied across the pn junction, the external field is in such a direction as to increase the internal junction field so that the drift component is increased. The diffusion of majority holes from p to n type and majority electrons from n to p type across the junction cannot occur.
2. However when minority electrons in the p type and minority holes in the n type via random motion reach the depletion region, the junction field pushes them across the junction. This results in a small current called the reverse saturation current whose conventional direction is from cathode to anode.
3. When the bias is sufficiently increased, the phenomenon of junction breakdown occurs which results in a large reverse current flow near the breakdown voltage.

Diode V-I Characteristics and current expression of diode:

1. The diode relation is $I = I_s (\exp(V/\eta V_T) - 1)$ where $I_s$isthe reverse saturation current and V_T is the thermal voltage (25 mV at room temperature). This equation excludes the breakdown region. Typically $I_s$is in nanoamperes and I in milliamperes.
   ηia a constant.Its value is 1 for Ge and 2 for si diodes.

   Temperature dependenciesof V-I characteristics of diode:
   The reverse saturation current (I_s)approximately doubles for every 10 degree Celsius rise in temperature due to thermal generation of electron-hole pairs.



2. V_T =kT/ e equates electric and thermal energy; e = electronic charge, k = Boltzmann constant in Joule/Kelvin is the conversion factor between temperature and energy, T in Kelvin is temperature in absolute scale.
3. Under forward bias, current starts to pick up only when the voltage is above the cutin value which is about 0.7 V for silicon and 0.3V for germanium. forward current is in mill amperes.

4. Under all circumstances, VI = diode power dissipation should not exceed the diode power rating or else diode will be destroyed due to excess heat.

Concept of junction capacitance:

1. Capacitance is defined for a system of two conductors separated by an insulator having equal and opposite charge for which the electric field between them and hence the potential difference between them is proportional to charge; capacitance = charge/voltage.
2. There are two capacitive effects in a diode: the junction capacitance in the depletion layer and the diffusion capacitance due to charge diffusion across the junction.
3. Across the depletion layer, there are fixed positive ions on one side and negative ions on the other and this configuration is like that of a capacitor. Under varying reverse bias the width of the depletion layer changes which changes the amount of charge and thus the capacitance changes. A class of diodes called the varactor diode uses this mechanism to realize variable capacitance.
4. Under forward bias, charge diffusion across the junction results in excess positive holes on the n side and excess negative electrons on the p side giving rise to a capacitive effect.

pn junction breakdown conditions: avalanche and zener breakdown

1. A large reverse current flows over a small interval centered around the reverse breakdown voltage. There are two mechanisms: avalanche and zener.
2. In the avalanche effect, electrons and holes constituting the reverse saturation current gain sufficient kinetic energy from the reverse field to rupture covalent bonds generating electron-hole pairs which in turn can rupture more covalent bonds thus generating a large number of charge carriers and hence current.
3. The zener effect occurs for junctions with high doping levels which results in a depletion layer of narrow width. Under high reverse bias the electric field is strong enough to rupture covalent bonds generating a large number of charge carriers. A class of diodes called the zener is operated in the breakdown region and is used as a source of reference voltage equal in value to the breakdown voltage.

Diode Application:

1. **Rectifier:** The directional current property of a diode is used for ac to dc conversion:ac supply (high ac voltage)□step down transformer (low ac voltage) □full wave rectification (ac to fluctuating dc) □ filter (dc by removing fluctuations, here using a capacitor which bypasses ac signals).
   The filter acting on the fluctuating dc, removes most of the fluctuations but a small part remains called ripple. To generate different dc voltages, different step down transformer ratios are used. In order to stabilize the dc voltage against

changes in ac voltage and load resistance, a circuit called a regulator follows the filter.

Diode half wave and full wave rectifier circuits:

In the half wave rectifier, the diode conducts (forward biased) only in the positive half cycle of the input signal and so only the positive half cycle appears at the output. In the full wave rectifier the two diodes conduct in alternate half cycles since with respect to the center tap, the anode potentials are opposite. The load current flows in one direction at all times.ie. unidirectional current flow through the load resistance.

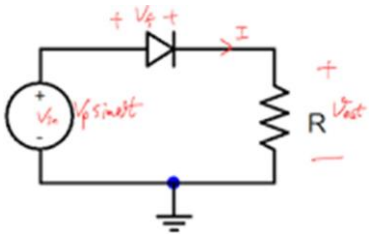


Fig: Half wave rectifier

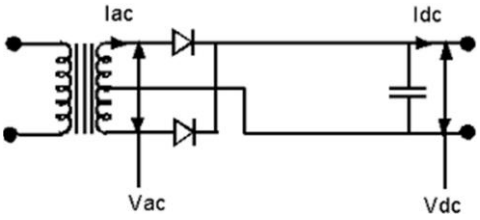


Fig: Full wave rectifier

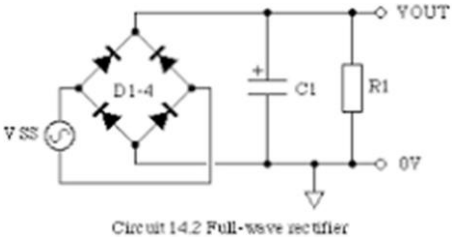
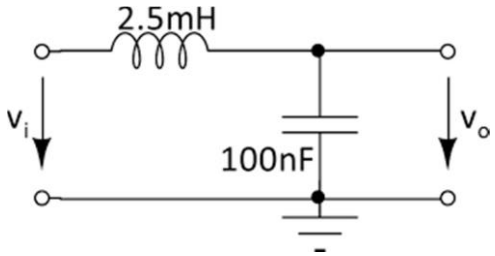


Fig: Bridge rectifier

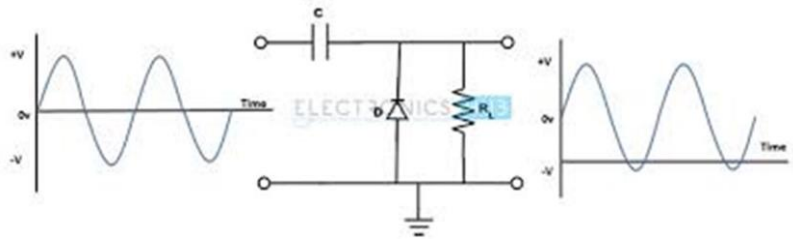
PIV: Peak Inverse Voltage – Maximum inverse voltage across the diode when it is not conducting.

Reduction of ac ripples using Filtercircuit:

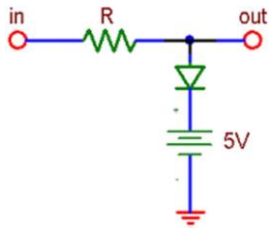
2. The circuit properties of the inductor and capacitor depend on the time rate of change (frequency) of signal. The i-v relation for an inductor is v (t) = L di(t)/dt and for the capacitor i(t) = C dv(t)/dt. A low pass filter blocks high frequency signals and passes low frequency signals. It is typically constructed using a series inductor followed by a shunt capacitor. The inductor drops ac voltage and the capacitor bypasses ac current and this combination realizes a low pass filter.



3. **Design of aclamper circuit**
   A clamper circuit is used to add a dc to an ac voltage. Since the diode conducts during the negative half cycle of the input, the capacitor charges to the input peak value resulting in output = input + (dc) peak using KVL.

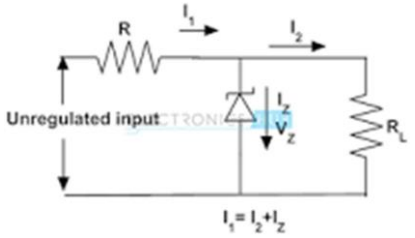


4. **Design of aclipper circuit**
   A clipper circuit limits the input ac voltage to some value below the+/-peak. In the circuit below, as long as the input is below +5 V, the output equals the input since the diode is reverse biased. If the input exceeds +5 V, the output equals +5V since the diode then conducts (output is clipped, diode drop neglected).



Zener diode and its characteristics & its use as a voltage regulator

5. A zener diode operated in the breakdown region is used as a voltage regulator. The breakdown voltage provides the constant load voltage.Load regulation: any variation in load results in varying load current, but since the input current remains constant, the difference in current is bypassed through the diode. Input regulation: if the input voltage changes, the input current changes but since the load current remains constant, the difference in current is bypassed through the diode.



Fig;Zener diode usedas a voltage regulator

Voltage doubler : Here output voltage = 2 x input voltage

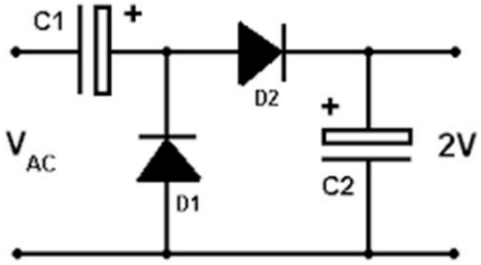


Fig: Voltage doubler

Miscellaneous:

1. A metal-semiconductor junction can be of two types: rectifying, ohmic. The rectifying junction acts like a diode; junction properties depending on relative distribution of electron energies between metal and semiconductor; for example, aluminium-n type acts like a pn junction. The ohmic junction is realized by heavy doping of the semiconductor in the region of contact with metal (n^{++} doping) to make it metal like and is used to bond metal terminals to the semiconductor resulting in electron conduction in both directions.
2. In a light emitting diode (LED), under forward bias, electrons combine with holes in the depletion region and the energy difference is emitted as light; the

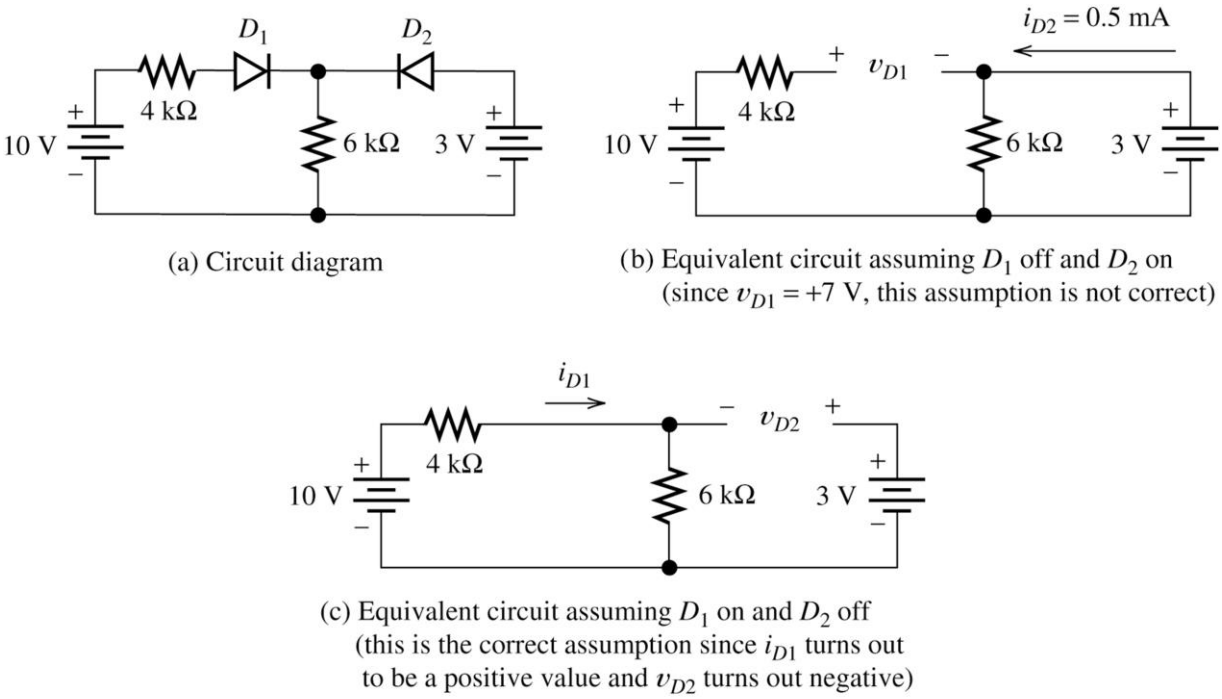
semiconductor used is the gallium arsenide family. In silicon, the energy difference is dissipated as heat.

3. The solar cell is a pn junction connected to a resistor. Photons in sunlight falling on the depletion region create electron-hole pairs by exciting electrons to break away from the covalent bond and the junction electric field drives the charge carriers to flow through the resistor thus converting sunlight to electricity.

Problem

Analyze the circuit shown below using the ideal diode model. Start by assuming the D1 is off and D2 is on.

Courtsey :www.ohio.edu/people/starzykj/.../Lecture5%20Diode%20Circuits.ppt



(a) Circuit diagram

(b) Equivalent circuit assuming D_1 off and D_2 on (since $v_{D1} = +7$ V, this assumption is not correct)

(c) Equivalent circuit assuming D_1 on and D_2 off (this is the correct assumption since i_{D1} turns out to be a positive value and v_{D2} turns out negative)

Figure 10.16 Analysis of a diode circuit using the ideal-diode model. See Example 10.5.

Courtsey :uav.ece.nus.edu.sg/~bmchen/courses/EG1108_Rectifiers.pdf

Problem 2 A 50 Ω load resistance is connected across a half wave rectifier. The input supply voltage is 230V (rms) at 50ΩA 50 Hz. Determine the DC output (average) voltage, peak-to-peak ripple in the output voltage (Vp-p), and the output ripple frequency (fr).

Solution:

The peak amplitude of the source voltage can be calculated as:Vm.= 230 ×√2 =325.3V

Output DC voltage: Vavg = Vm/π= 103.5 V.

The peak-to-peak ripple voltage is the difference between the maximum and the minimum in the vo waveform. 325.3V – 0 =Vm - 0=Vp-p.

Therefore, Percentage ripple = (Vp-p/Vavg) x 100 = 314%.

Note: The ripple is at the supply frequency of 50 Hz. We notice that the "percentage ripple" is 314%, which is very large, and undesirable. This ripple can be reduced by adding a capacitor across the load resistor. The capacitor acts to filter (reduce) the ripple voltage, as we will see later.

Problem 3.The reverse saturation current at 300K of a pn junction diode is 5 µA.Find the voltage to be applied across the junction to obtain a forward current of 50 mA.

Solution: Use diode current eqn; $I = I_s (\exp(V/ \eta V_T) – 1)$

Given I= 50 mA, Is = 5 µA, T=300K

So we get, V = 0.238 V

Exercises:

1. Compare dc (V/I) and ac (dV/dI) resistance of a diode using the diode equation. Show that the ac resistance at room temperature is about 25 mV/I. These resistances thus depend on the dc operating point on the diode characteristics.
2. For the zener regulator circuit above, input 20 V, $V_z = 10$ V, $R = 220\ \Omega$, $R_L = 180\ \Omega$, determine the circuit currents. (Hint: $I_{in} = (V_{in} – V_z)/R$, $I_L = V_z/R_L$, $I_Z = I_{in} – I_L$.)
3. Draw the circuit of a Half wave,full wave (centre tap type) and full wave bridge rectifier. Explain its working principle and input, output waveforms.
4. In the clamper circuit above, show that if the diode is reversed, output = input – (dc) peak using KVL and sketch the output. In the clipper circuit above, if the battery is reversed, sketch the output for a sinusoidal input.
5. In a dc power supply, a capacitor filter is often used. Explain its working
   a) graphically b) using its circuit relation
   (hint: i=Cdv/dt, v might be small but dv/dt can be large).

6. Explain the effect of temperature on the reverse saturation current of a diode.

7 Fill in the blanks:
   a) For the same forward diode voltage, if the junction area is increased, current ____.
   b) A resistor is placed in series with a diode to ___.

c) In the diode equation, for $V/V_T<<1$, expanding the exponential gives ___.
d) The switched mode power supply (SMPS) differs from a diode rectifier based power supply in that ___.
e) A low pass filter has a capacitor in parallel since ___.

8. MCQ

i) To design a bridge rectifier, no of diodes required is

a) 1 b) 2 c)3 d)4

ii) The depletion region width of a pn diode is about

a) 0.5 cm b) 0.5mm c) 0. 5 μm d) 0.5 nm

iii) The cutin voltage of Ge diode is

a) 0.3 V b) 1.1 V c) 0.7V d) 5V

iv) A rectifier converts

a) Ac signal to dc signal b) dc signal to ac signal c) None of these

v) Which dide can emit light

a) Zener diode b) Rectifier diode c) LED d)Schotky diode

vi) Azener diode can be used in

a) Forward bias only b) reverse bias only c) Both forward and reverse bias d)None of these

vii) The value of V_T at room temp (300K) is

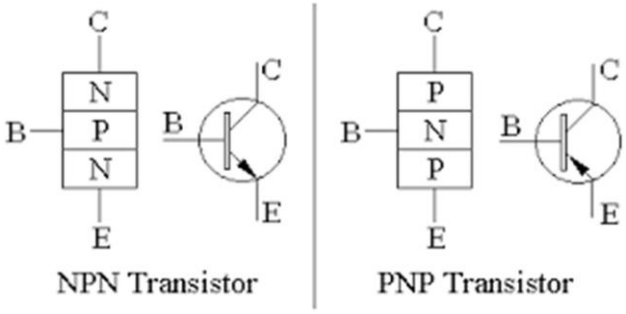
a) 26 mV b) 0.3 V c) 0.7 V d) 1.1 V

Module I
PART 3: BIPOLAR JUNCTION TRANSISTOR 6L

Introduction: A semiconductor pn junction based three terminal device in which one terminal is used to control the current flow between the other two terminals. There are two classes of transistors: bipolar junction transistor (BJT) and field effect transistor (FET). In the BJT, the control signal is a current and in the FET, the control signal is a voltage. The transistor can be used either as an Amplifier: small changes in the control signal lead to large changes in the controlled current or as a Switch: control signal is used to turn the controlled current ON/OFF.

Formation of npn/pnp transistors:

1. It has two pn junctions with structure pnp or npn, in sequence called emitter (E), base (B), collector (C). Doping: the emitter is heavily doped, the base lightly doped, the collector moderately doped; Size: the EB junction area is moderate, the width of the base is narrow, the BC junction has large area.



Junction biasing condition for active, saturation, cut off modes:

2. The two pn junctions can be biased in different combinations giving the modes of operation: active – EB junction forward biased, BC junction reverse biased, saturation - EB, BC junctions forward biased, cut off – EB, BC junctions reverse biased.
3. As an amplifier the active mode is used and as a switch the saturation/cut off modes are used.
4. There are three configurations based on the terminal common to input and output: common emitter (CE) - emitter is common, common base (CB) – base is common, common collector (CC) – collector is common. The npn, CE combination is mostly used.
5. The **static characteristics** of the transistor (npn, CE) are the input: I_B vs V_{BE} with V_{CE} as parameter, output: I_C vs V_{CE} with I_B as a parameter.

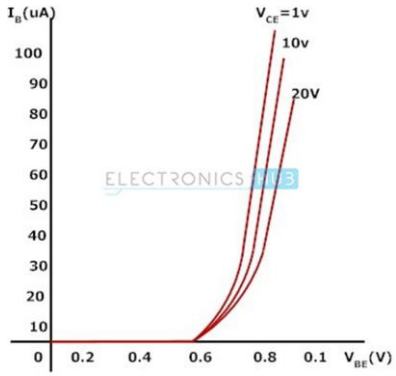


Fig: Input Characterristics

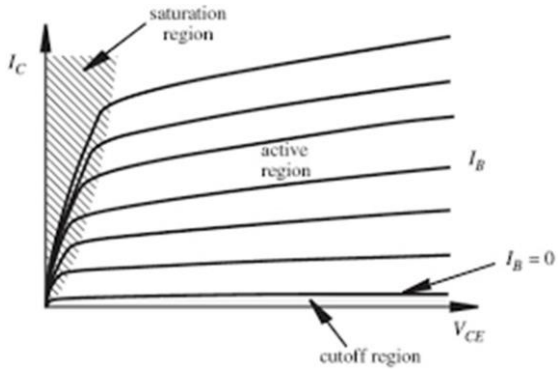


Fig: Output Characterristics

Transistor (npn) Action- current conduction mechanism:

1. Assume EB junction forward biased, BC junction reverse biased. Due to forward bias, across EB junction, large number of electrons move from n to p and few holes from p to n due to doping difference, which is the main constituent of the emitter current.
2. Since base is lightly doped and narrow, few electrons combine with holes in the base and most reach the depletion layer of the reverse biased BC junction where the strong electric field is in such a direction as to pull the electrons into the collector, that is, although the BC junction is reverse biased, a large current crosses the junction. This is the main constituent of the collector current.
3. If a resistor is connected to the collector terminal, the collector current is independent of its value (contrary to experience wherein current changes as resistance changes).
4. The holes lost in the base is supplied from the external circuit via the base terminal as the base current.

BJT Current Gain α, β:

5. The current relationship is $I_E = I_B + I_C$. The ratio I_C/I_E is the transistor α (a value nearly 1) and $I_C/I_B$is the transistor β (a value larger than 1) [$\beta = \alpha/(1-\alpha)$]. These ratios are similar even for increments, that is, βac = βdc.

Early Effect

As the reverse bias of rthe collector junction is increased, the effective base width decreases.This is known as base width modulation or early effect.

BJT Configurations-CE, CB, CC:

(CE-Common Emitter, CB-Common Base, CC-Common Collector)

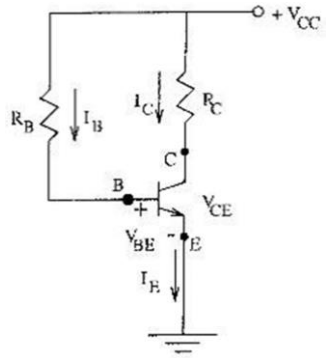
The CC configuration has large input resistance, low output resistance, voltage gain of unity, large current gain and power gain. It is used as a buffer for connection of another amplifier to a low resistance load which would otherwise reduce the amplifier gain.

1. The CB configuration has low input resistance, large output resistance, current gain of unity, large voltage gain and power gain.
2. The CE configuration has moderate input and output resistance, moderate voltage, current and power gain. It is widely used.

Biasing and bias stability:

BJT (npn, CE, active mode)

1. With the help of dc supply and resistors (biasing circuit) the transistor is properly biased to establish a dc operating point in the center of the active region.
2. BJ biasing circuits:**fixed bias, voltage divider bias&collector to base bias**shown below.



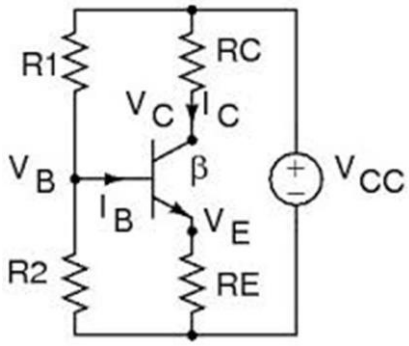


Fig:fixed bias circuit **Fig:voltage divider bias circuit**

Fixed bias circuit: the input side equation is $V_{CC} = I_B R_B + V_{BE}$ (=0.7 V) and the output side equation is $V_{CC} = I_C R_C + V_{CE}$. From the first equation I_B is found and from the second V_{CE} using $I_C = \beta I_B$. Since $V_{CE} = V_{CB} + V_{BE} = -V_{BC} + V_{BE}$, it should be verified that $V_{BC} < 0$ for active mode.

3. Sometimes a resistor is included in the emitter lead. This is done to stabilize the dc operating point against temperature fluctuations using negative feedback. If the temperature rises (falls), the collector current rises (falls) due to increase (decrease) in reverse saturation current in the reverse biased BC junction; this increases (decreases) the emitter voltage which decreases

(increases) the BE voltage which decreases (increases) the collector current.

4. The dc operating point is defined by the values of I_B, V_{BE} on the input side and I_C, V_{CE} on the output side.
5. The biasing resistors on the input side are in general large to limit I_B (microamperes) and moderate on the output side to limit I_C(mill amperes) and achieve gain.

Stability factors (S) for different biasing circuits:

Stability factors (S) is defined as

S = $\delta I_C/\delta I_{co}$when V_{CE} remain constant.

where Ic= collector current,I_{co} = reverse saturation current, V_{CE} = Collector Emitter voltage.

1. Fixed Bias Circuit: S = β+1
2. Collector-to-base bias circuit : S = [β+1] / [1+ R_L/(R_B +R_L)]
3. Voltage Divider Bias : S = (β+1)(1+R_T / R_e) / (1+ β+R_T / R_e)

where RB = Base Resistance, Re = Emitter Resistance, R_L = Load Resistance

R_B = Thevenin Equivalent Resistance = R_1R_2 / R_1 + R_2

BJT (npn, CE, active mode): Amplification

1. Qualitatively the amplification can be described as follows. The small ac signal to be amplified is applied on the input side to the BE junction. The BE junction has diode characteristics: due to the exponential equation, small changes in junction potential leads to larger changes in junction current. The larger change in base current leads to large change (β times) in collector current which through the collector/load resistor leads to large change in collector voltage. The small ac input leads to large ac output and thus amplification.
2. In the amplifier C1, C2 are coupling capacitors which allow ac currents to flow (capacitor easily charges and discharges) to allow ac signals to be coupled to the amplifier/load resistor and blocks dc currents (capacitor charges and then current stops) to isolate input/output from the dc supply. The capacitor CE is a bypass capacitor which effectively shorts the resistor in parallel for ac but not for dc. The ac signal to be amplified is applied at the input (base-emitter) side and the amplified signal is obtained at the output (collector-emitter) side.

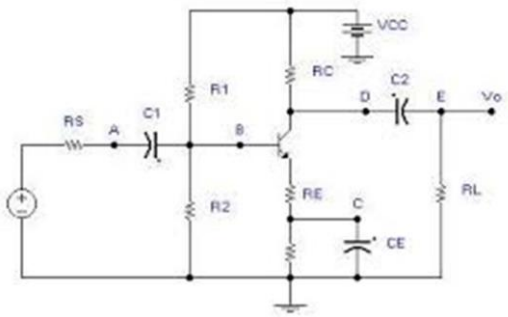


Fig RC coupled transistor amplifier circuit

DC load line and Q point:

The amplification process can be explained graphically. The dc operating point is chosen to lie in the middle of the active region. The dc collector current and voltage are constrained by the output circuit and satisfy a KVL equation. This equation plotted on the output characteristics is the load line (a straight line) passing through the dc operating point. The ac signal fluctuates about the dc operating point along the load line. As seen from the characteristics, changes in base current on the order of microamperes lead to changes in collector current on order of mill amperesand to changes in collector-emitter voltage in volts. The ac swing about the dc point is restricted to the active region.

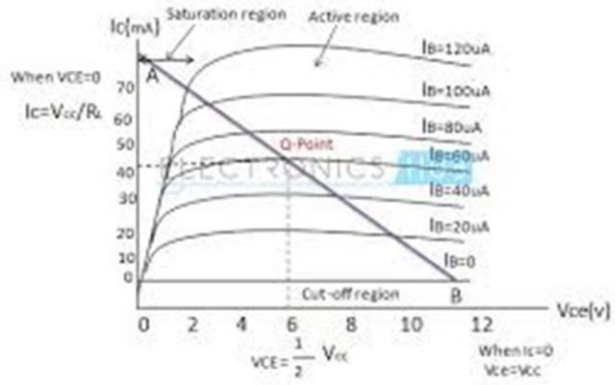
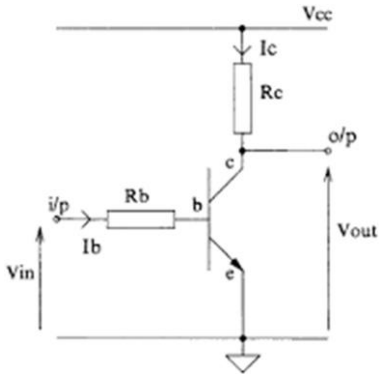


Fig : DC load line and Q point

BJT (npn, CE): Switch:

1. In the saturation region, the EB and BC junctions are forward biased. Since $V_{CE} = V_{CB} + V_{BE} = -V_{BC} + V_{BE}$ and both of the order of 0.7 V, V_{CE} is close to zero. Thus the collector current is constrained by the external circuit and not the transistor and is the maximum possible, that is, it saturates. If in the active mode, the EB junction is driven hard and I_B large enough, I_C is large enough so that the drop in the collector resistor is large enough to reduce the collector potential to a value below the base potential thus achieving saturation.
2. In the cut off region, both junctions are reverse biased so no current flows in the transistor.
3. A BJT is operated as a switch, ON/OFF, when driven between saturation and cutoff by a voltage pulse applied at the base.



Courtesy: www.ohio.edu/.../Lecture13%20**BJT**%20Transistor%20Circuit%20Analy.

Problem 1

Analyze the circuits shown in Figure P13.45 to determine I and V. For all transistors, assume that β = 100 and $|V_{BE}| = 0.7V$ in both the active and saturation regions. Repeat for β = 300.

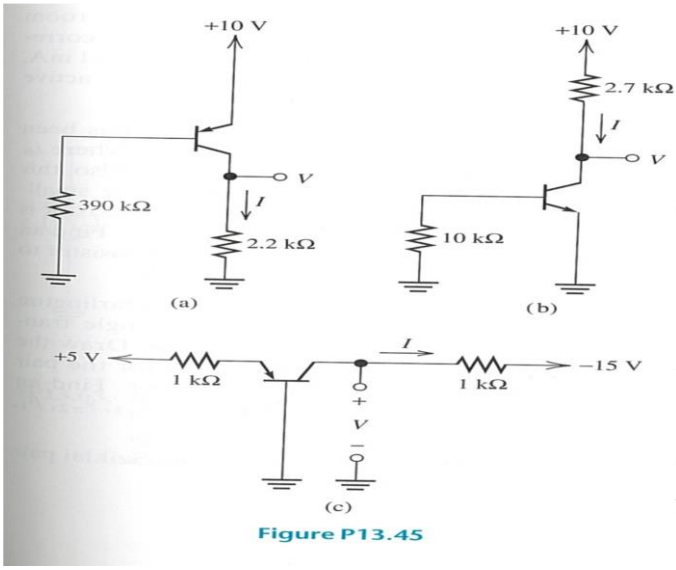


Figure P13.45

(a) for $\beta = 100$

$|V_{BE}| = 0.7 \quad => \quad V_B = 9.3V$

$$I_B = \frac{9.3}{390k} = 23.8\mu A$$

$I_C = \beta I_B = 2.38mA \quad => \quad V = I_C * 2.2k = 5.236\,V$

for $\beta = 300$

$I_C = 7.15mA \quad => \quad V = I_C * 2.2k = 15.73V$ (Incorrect)

Since $V_{max} = 9.8V \quad => \quad I_{C\max} = \frac{9.8}{2.2k} = 4.43mA$

$$=> \beta_{max} = \frac{I_{max}}{I_B} = \frac{4.42mA}{23.8\mu A} = 187.2$$

Problem 2

A transistor (CE configuration) having α=0.975 and reverse saturation current (I_{co})10µA .Find If the base current is 250 µA, calculate the emitter current and the collector current.

Solution: $\beta = \alpha/(1-\alpha)$.

Given α =0.975. So β = 39. ,base current I_B = 250 µA

So collector current $Ic = \beta I_B + (1+\beta)I_{co}$ = 10.2 mA.

emitter current $=I_E = Ic + I_B$ =10.4 mA

Exercise:

1. Study the reasons for classifying
   a) a source as either a voltage or current source
   b) an amplifier as either a voltage or current amplifier.
2. In the voltage divider bias circuit shown above, V_{CC} = 18 V, R_1 = 39 KΩ, R_2 = 8.2 KΩ, R_C = 3.3 KΩ, R_E = 1 KΩ, β = 120. Assuming V_{BE} = 0.7 V, find V_{BC}< 0 (active mode).
3. In the CE output characteristics shown above, estimate β (dc) = I_C/I_B at the Q point (dc operating point), and β (ac) = $\delta I_C/\delta I_B$ about the Q point when I_B changes from 40 to 80 µA.
4. In the BJT switch circuit shown above, $V_{CE} = V_{CC} - I_C R_C$. If I_C is sufficiently large, V_{CE} is nearly 0 V and V_{BC}> 0, that is, the transistor is in saturation. To make I_C large, I_B must be high, that is, the base should be driven hard (in saturation, the relation $I_C = \beta I_B$ does not hold). If V_{CC} = 5 V and R_C = 1 KΩ, find I_C (saturation).
5. Derive the expression of stability factor S for 3 biasing circuit. Compare the result.
6. Fill in the blanks:
   a) In an amplifier, the Q point is in the middle of the active region to ensure ____.
   b) When a BJT enters saturation, value of V_{CE} is ____.
   c) In a CE amplifier, if the base voltage rises, collector voltage falls; the reason being ____.
   d) In a CC amplifier, the input is applied at the base and output is taken at the emitter. It is called emitter follower since ____.
   e) In a CB amplifier, the input resistance is low and the output resistance is high since ____.

MCQ

7.

i) A BJT has

a) 3 terminals and 2 junctions a) 3 terminals and 3 junctions

c) 4 terminals and 2 junctions d) a) 2 terminals and 2 junctions

ii) In a npn BJT

a) Electron is majority carrier and hole is minority carrier

b) Electron is minority carrier and hole is majority carrier

c) None of these

iii) In active mode of BJT biasing

a) E-B junction is forward biased and C-B junction is reverse biased
b) E-B junction is reverse biased and C-B junction is forward biased
c) Both E-B junction and C-B is forward biased
d) Both E-B junction and C-B is reverse biased

iv) The best biasing circuit is (Lowest value of Stability factor S)

a) fixed bias
b) voltage divider bias
c) collector to base bias
d) None of these

v) The relation between α and β of a BJT is

a) $\beta = \alpha/(1-\alpha)$ b) $\beta = \alpha/(1+\alpha)$ c) $\alpha = \beta/(1-\beta)$ d) None of these

Module -II: Field Effect Transistor (FET) 4L

2.1 Introduction

The Field Effect Transistor (FET) is a semiconductor device. In FET out put current is controlled by input electric field. For this reason FET is known as Filed Effect Transistor. As output current is controlled by input field FET is one example of voltage controlled current source.

In case of BJT as already discussed output current is controlled by input current .Therefore BJT is basically current controlled device.

Contrast to BJT, in FET current is carried by only one type of carriers (Either Electrons / Holes). For this reason FET is known as unipolar device.

2.2 Classification, Construction of JFET, Operating Principle

2.2.1 Classification of FET

FETs are classified as followings. FETs are in two group – Junction Field Effect Transistor (JFET) and Metal Oxide Semiconductor Field Effect Transistor(MOSFET) . JFET again two types – n-channel JFET and p-channel JFET . MOSFET can be classified in two groups – Depletion-Enhancement MOSFET (DE-MOSFET) or simply known as Depletion MOSFET (D-MOSFET) and Enhancement only or E-Only MOSFET or simply known as E-MOSFET . DE-MOSFET again two types – n-Channel DE-MOSFET and p-channel DE-MOSFET. Also E-MOSFET two types – n-channel E-MOSFET and p-channel E-MOSFET. The classification is also shown in Fig.2.1.

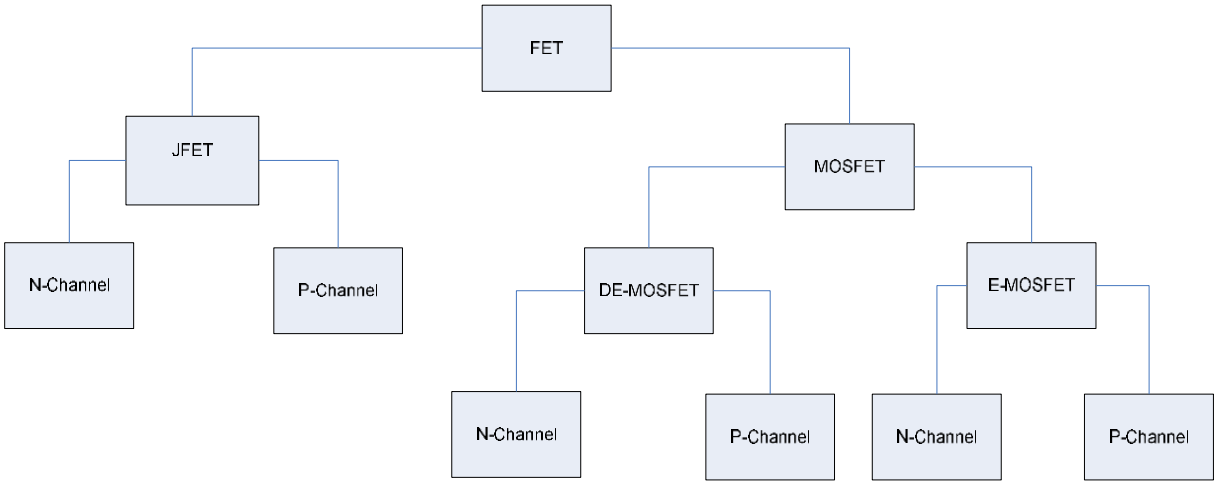


Fig. 2.1: Classification of FET

2.2.2 Construction of JFET

The schematic view of construction of n-channel JFET is shown in Fig. 2.2. There are three terminals in the structure namely (i) Drain (D) (ii) Gate (G) (iii) Source (S) .

For high frequency shielding another terminal also used in actual physical structure of JFET.

For n-channel JFET, channel is n-type material. Gate material is opposite to channel type i.e. for n-channel JFET; channel is p-type material. Gate region is heavily doped compared to channel. Here P^+ indicates heavily doped region with p-type material. In the schematic structure (Fig.2.2), channel region is belonging between gate regions. Metal contacts are employed for terminal contact i.e. to connect the device with circuitry. As shown in the diagram (Fig. 2.2) the JFET structure is symmetrical. Basically all the FETs structure is symmetrical.

For p-channel JFET all the doping type would be replace by opposite type. This means channel is p-type; gate region is n-type heavily doped. The electrical symbol JFET is shown in Fig.2.3.

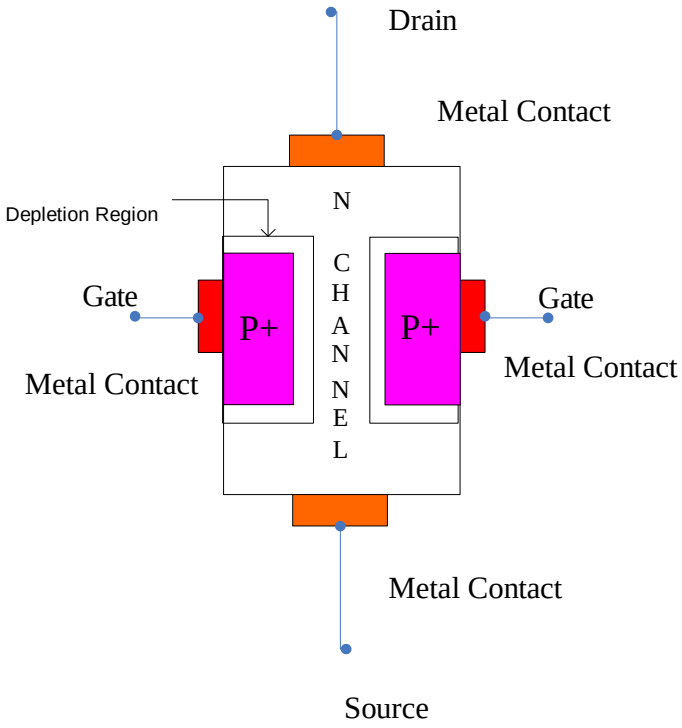


Fig.2.2: Construction of N-Channel JFET

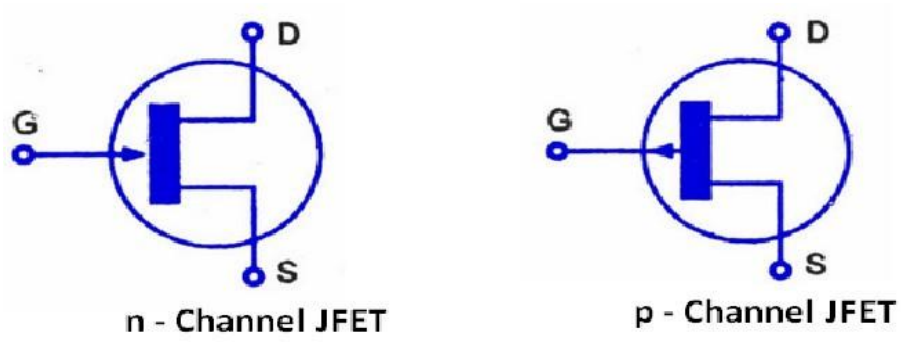


Fig . 2. 3 : Electrical Symbol of JFET

2.2.3 Operation of JFET

The fig.4.4 shows the circuit of n-channel JFET with normal polarities. The two p-n junctions at the sides form two depletion layers. The current conduction by charge electrons is through the channel between the two depletion layers and it goes out of the drain. The width and hence resistance of this channel can be controlled by changing the input voltage V_{GS}. The greater the reverse voltage V_{GS}, the wider will be the depletion layer and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen when V_{GS} decreases. Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}. In other word, the magnitude of drain current I_D can be changed by altering V_{GS}

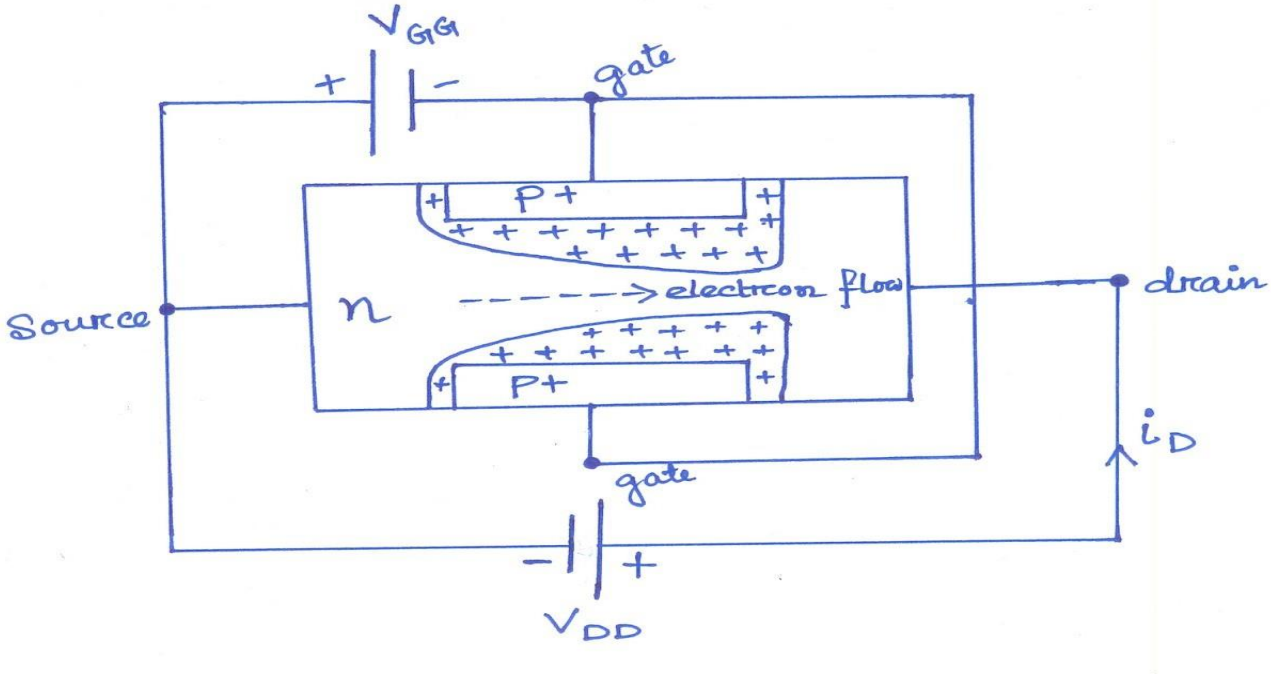


Fig. 2.4 : Biasing arrangement for current through n-channel JFET

The working of JFET can be explained as follows:

Case-I :

When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero, the two p-n junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of the depletion layers determines the width of the channel and hence current conduction through the bar.

Case-II:

When a reverse voltage V_{GS} is applied between gate and source terminals, as shown in fig.2.5, the width of depletion layer is increased. This reduces the width of conducting channel, thereby increasing the resistance of n-type bar. Consequently, the current from source to drain is decreased. On the other hand, when the reverse bias on the gate is decreased, the width of the depletion layer also decreases. This increases the width of the conducting channel and hence source to drain current. A p-channel JFET operates in the same manner as an n-channel JFET except that channel current carriers will be the holes instead of electrons and polarities of V_{GS} and V_{DS} are reversed.

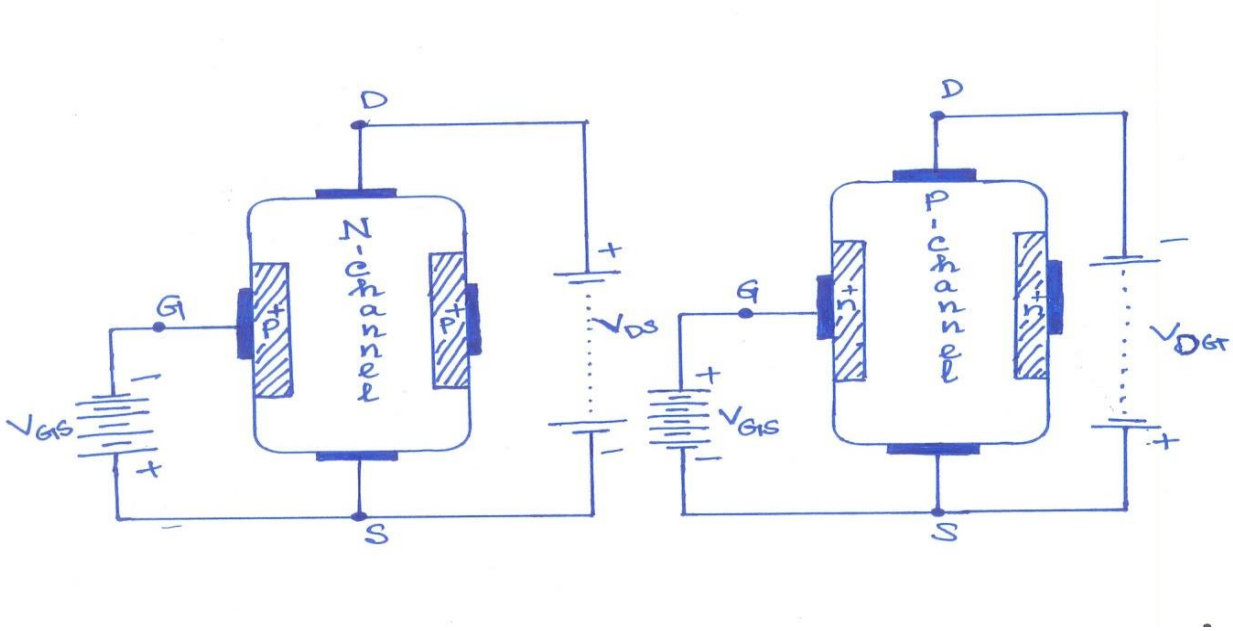


Fig .2.5: Polarity Convention

2.2.4 Drain and Transfer Characteristics of n-channel JFET

I. V_{GS}=0 V ,V_{DS}=0 V

When neither any bias is applied to the gate (i.e. when V_{GS} = 0) nor any voltage to the drain w.r.t. source *(i.e.* when V_{DS} = 0), the depletion regions around the p-n junction, are of equal thickness and no current through the device as shown in fig.2.6.a.

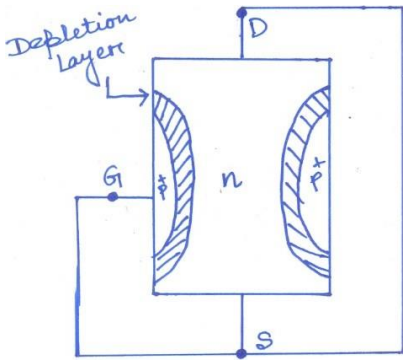


Fig 2.6.a: V_{GS}=0 V and V_{DS} = 0 V

II . V_{GS}=0 V and V_{DS} is increasing from zero Volt

When positive voltage is applied to the drain terminal -D w.r.t. source terminal S keeping V_{GS}=0 i.e gate is shorted to source as illustrated in fig. 2.6.b , the electrons (which are the majority carriers) flow from terminal S to terminal D whereas conventional drain current I_D flows through the channel from Drain to Source. Due to flow of this current, there is uniform voltage drop across the channel resistance as we move from terminal D to terminal S. This voltage drop reverse biases the diode (p-n junction between gate to channel) . The gate is more "negative" with respect to those points in the channel which are nearer to D than to S. Hence, depletion layers penetrate more deeply into the channel at points lying closer to D than to S. Thus wedge- shaped depletion regions are formed, as shown in fig.2.6.b. The size of the depletion layer formed determines the width of the channel and hence the magnitude of current I_D flowing through the channel. As V_{DS} is increasing current is also increasing almost linearly. When V_{GS} is 0 V , at some critical voltage of V_{DS} , depletion regions from both side of the device meet near to drain end this phenomenon is known as pinch-off (Fig . 2.6.c) .

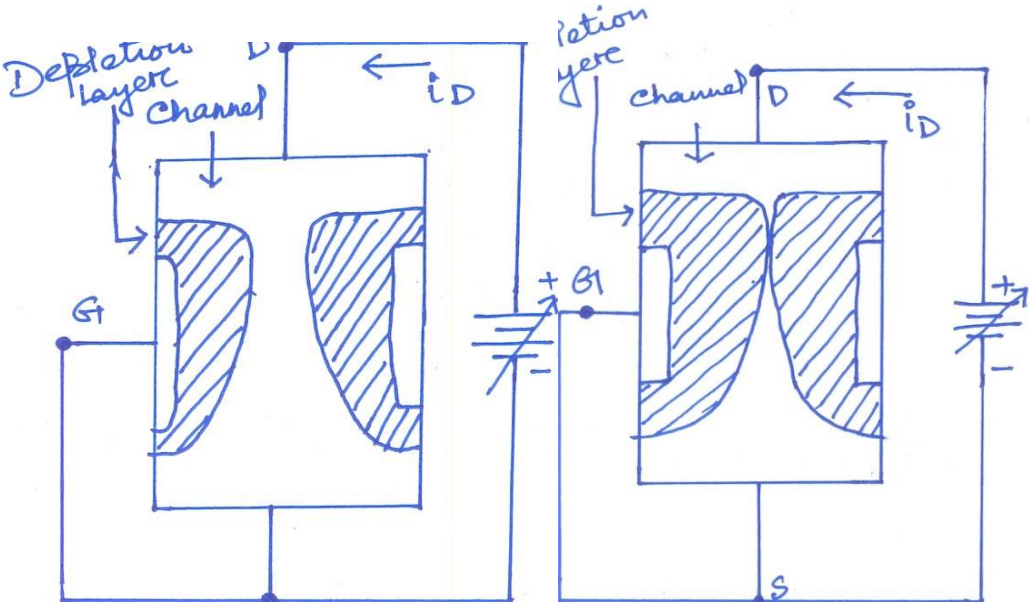


Fig . 2.6. b : Increasing of depletion region

Fig.2.6.c. : Pinch-off phenomenon

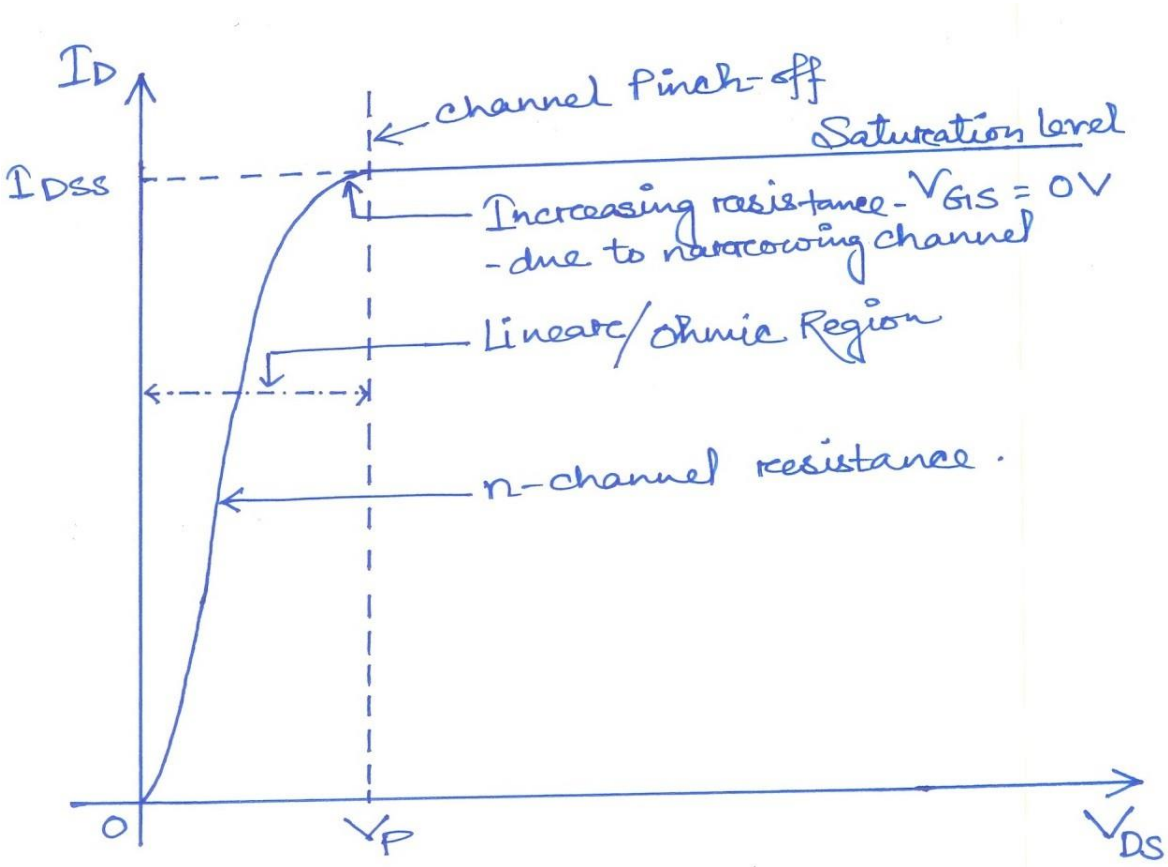


Fig . 2.6. d . : Drain Characteristics at for V_{GS} = 0 V

So as seen from figure 2.6.d for V_{GS}=0 V , whenever V_{DS} is increasing from zero to higher voltage initially current increases linearly . However after channel pinch-off current no more increases but saturates. Graphically pinch-off voltage can be defined as follows when V_{GS} is zero the value of V_{DS} after which current saturates is known as pinch-off voltage (V_P) .

III. V_{GS} = -Ve and V_{DS} is increasing from zero Volt to positive direction

If gate is maintained at negative potential (Fig. 2.7) and V_{DS} is increasing from zero voltage, then depletion width is controlled both by V_{GS} and V_{DS} . With increasing V_{DS} from zero voltage current increases linearly and saturates after pinch-off .

If V_{DS} is increasing more and more in saturation region due to p-n junction break down current increases sharply and device will damage. For different values of V_{GS} family of drain characteristics is shown in figure 2. 8 . As seen from the curve as V_{GS} is decreasing from 0 to more negative value , saturation current is also decreasing. This indicates with changing input field output current has been controlled. So the name filed effect transistor.

Graphical determination of transfer characteristics: **I f** saturation current is plotted for particular value of V_{GS}, transfer characteristics is obtained as shown in fig . 2.8. If is seen that if V_{GS} reaches to pinch-off value no current flows through the device. And device enters into cut-off region.

So there are four region in drain characteristics (i) Linear /Ohmic region (ii) Saturation Region (iii) Cut-off region (iv) Break-down region .

Please note: If JFET enters into breakdown region it will damage.

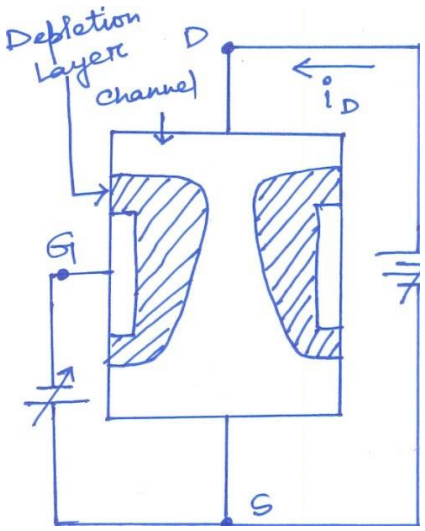


Fig . 2.7.: Gate is at negative potential and V_{DS} is increasing from zero voltage

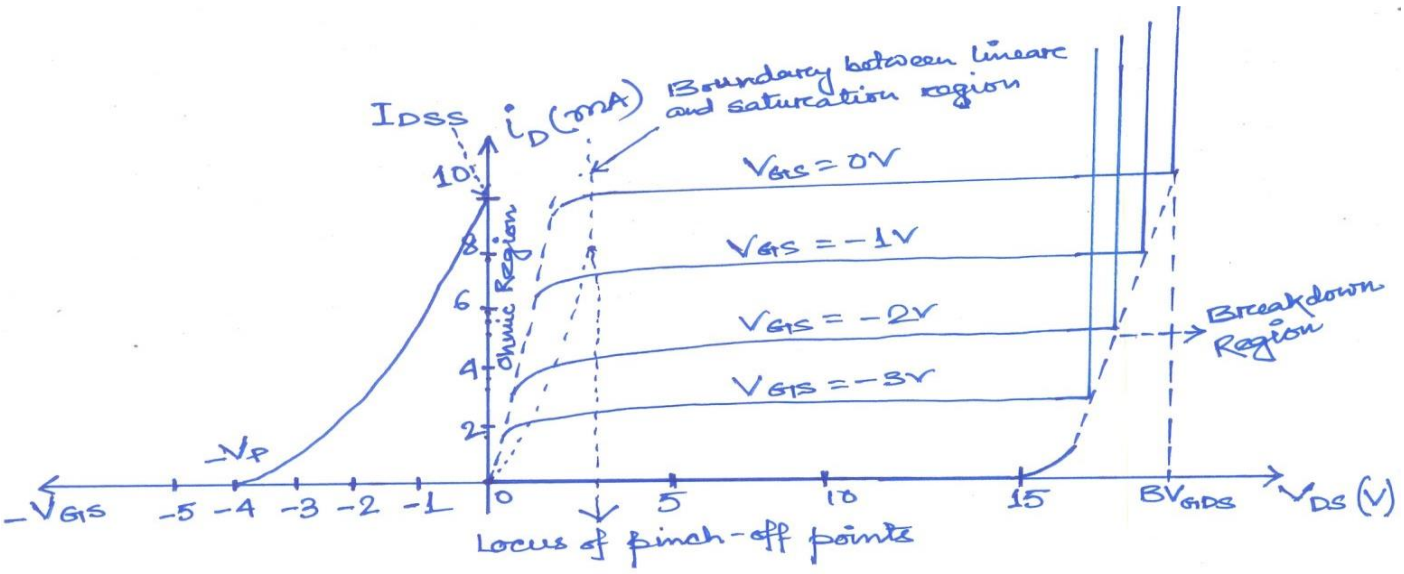


Fig. 2.8: Drain (1st Quadrant) and transfer characteristics (2nd Quadrant) of n-channel JFET

IV . V_{GS} = +Ve and V_{DS} is increasing from zero Volt to positive direction

If V_{GS} is maintained at positive potential with respect to source due to forward biasing of gate to channel junction field controlled action will be terminated.

2.3 Relation among JFET parameters

FET Parameters:

The drain current (I_D) is a function of the gate- source voltage(V_{GS}) and the drain –source voltage (V_{DS}). When we do the small-signal applications, i.e. when these quantities vary by small amounts about the quiescent values the ac component of the drain current i_d can be expressed in term of a linear combination of the ac components of the v_{gs} and v_{ds}. Thus,

$$i_d = g_m v_{gs} + (v_{ds}/r_d) \qquad (2.1)$$

$$\text{so,} \quad g_m = [\, i_d / v_{gs} \,] \,|_{vds=0} \qquad (2.2)$$

The parameter g_m is the mutual conductance or the transconductance or the common- source forward transconductance of the FET. The unit of g_m is Siemens (S), mho (Ω^{-1}) or A/V. It is defined as the ratio of the change in the drain current to the corresponding change in the gate- source voltage for a constant drain- source voltage. g_m is given by the slope of the transconductance characteristic.

$$r_d = (v_{ds} / i_d) \,|_{vgs=0} \qquad (2.3)$$

r_d is known as the ac drain or channel or output resistance of the device and is expressed in ohm. It is defined by the change in the drain-source voltage to the corresponding change in the drain current for a constant gate-source voltage. The reciprocal of rd is denoted by gd which is the drain or the channel conductance or the common –source output conductance. g_d is the slope of the drain characteristic.

The amplification factor μ gives the third parameter of the FET. The amplification factor is the ratio of the change in the drain –source voltage to the corresponding change in the gate-source voltage for a constant drain current.

$\mu = -\ (v_{ds} / v_{gs}])_{\ id=0}$ (2.4)

the negative sign arises since v_{ds} and v_{gs} have opposite signs for $i_d = 0$ (I_D = constant) and μ is a positive quantity.

From equation (2.1) with $i_d=0$

$$-(v_{ds}/ v_{gs}) \mid_{id = 0} = r_d\, g_m$$

or, $\mu = r_d\, g_m$ (2.5)

2.4 Common Source JFET Amplifier

In the Common Source FET amplifier a voltage divider biasing circuit with the resistors R_1 and R_2 has been used to establish the operating point or Q- point. The coupling capacitors C_1 and C_2 and the bypass capacitor C_s act as ac shorts. R_L is used as the load resistance. The input voltage v_i is applied between the gate and the ground, and the output ac voltage v_o is taken between the drain and the ground. As the source terminal is at the ground potential for ac voltages, the source is the common terminal between the input and the output, accounting for the name of the configuration.
Here, $v_i = v_{gs}$ and $v_o = v_{ds}$

The operation of the amplifier can be understood using following circuit .

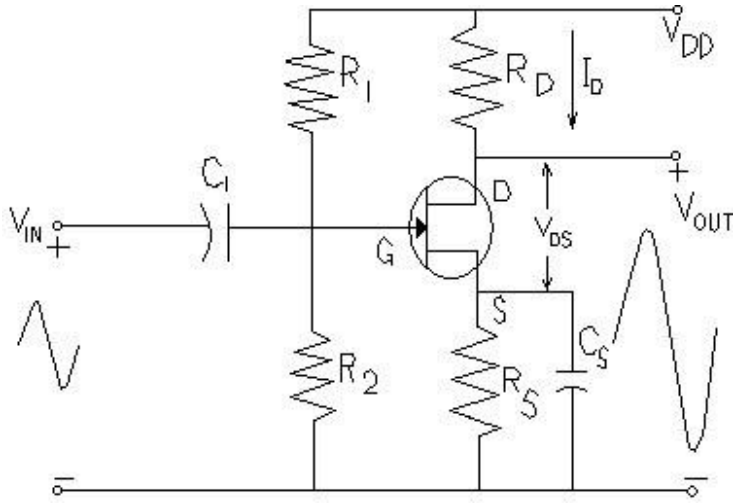


Fig. 2.9: Circuit of Common Source Amplifier

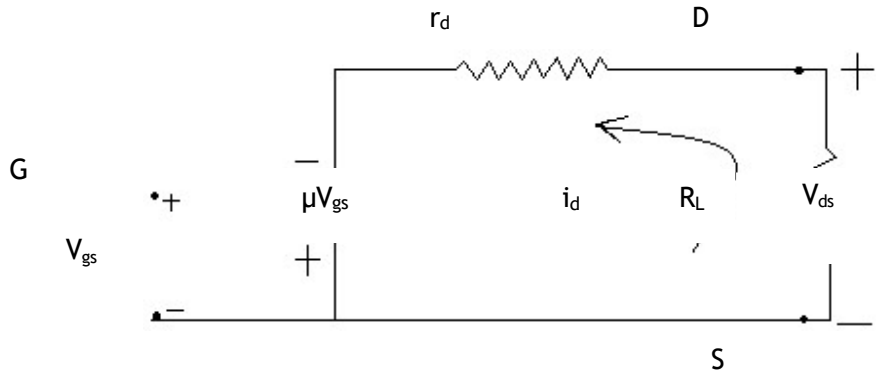


Fig. 2.10 Ac equivalent circuit of the Common Source amplifier

The voltage gain of the circuit can be derived as follows

Voltage Gain:

We apply, KVL,

$\mu V_{gs} = i_d (R_L + r_d)$ (2.6)

The output voltage is

$V_{ds} = - i_d R_L$ (2.7)

The negative sign is due to reference polarity of v_{ds} and the direction of i_d.

From eqn. 2.6 and 2.7 we write

$Vds = - (\mu v_{gs} R_L) / (R_L + r_d)$

So that the voltage gain is

$$A_v = v_{ds} / v_{gs} = - (\mu R_L) / (R_L + r_d) \qquad (2.8)$$

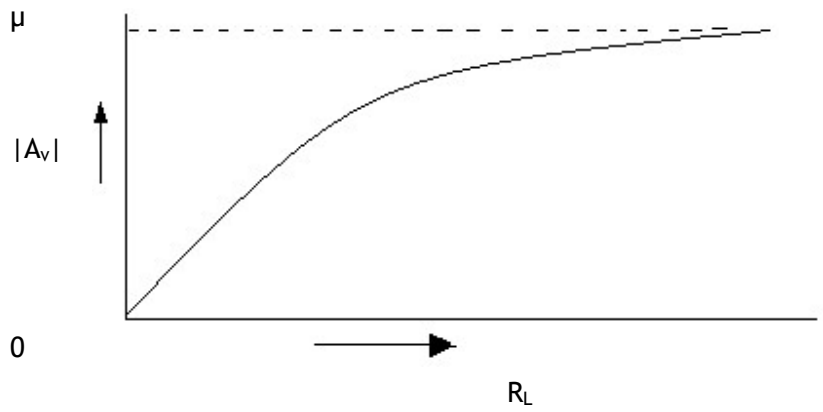


Fig. 2.11: $|A_v|$ versus R_L

In reality , R_L is smaller compared to r_d

Therefore equation 4.8 can be written as

$$A_v \approx - \mu R_L / r_d = - g_m R_L \qquad (2.9)$$

2.5 Common Drain Amplifier using FET

The circuit diagram of common drain amplifier is shown in fig. 2.12 .

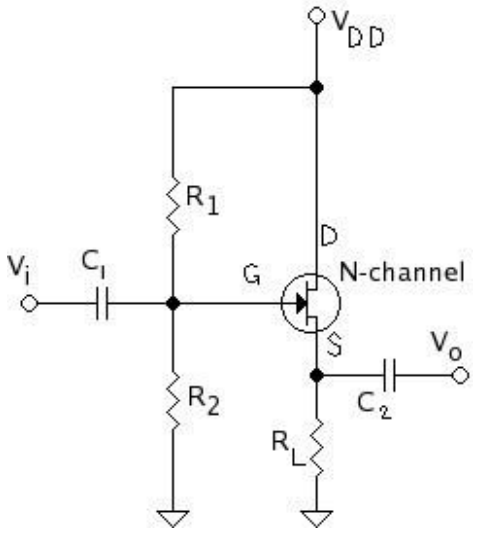


Fig. 2.12 : Common Drain amplifier

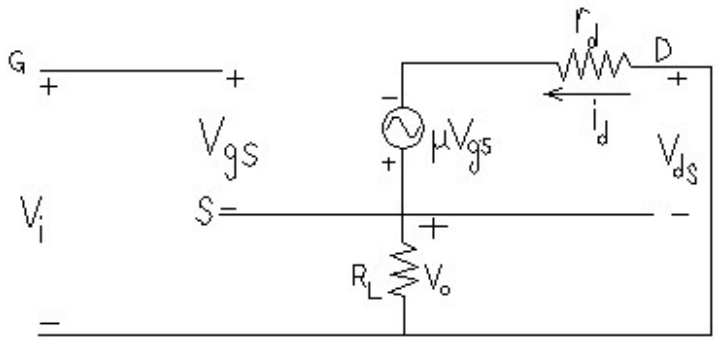


Fig. 2.13: A.C . Equivalent circuit of the common drain amplifier

Voltage gain of the common drain equivalent circuit of fig.2.13 can be determined as follows

We know $v_{ds} = i_d r_d - \mu v_{gs}$ (2.10)

$v_i = v_{gs} + v_o$ (2.10a)

$v_o = i_d R_L$ (2.11)

$v_{ds} + v_o = 0$ (2.12)

Eqn 2.10 and 2.12 we get

$v_o = - v_{ds} = - i_d r_d + \mu v_{gs}$

$= - (v_o r_d) / R_L + \mu (v_i – v_o)$ (2.13)

Rearranging we obtain

$v_o (1 + r_d/ R_L + \mu) = \mu v_i$

So, the voltage gain is

$A_V = v_o/v_i = (\mu R_L) / [(\mu+1) R_L + r_d]$ (2.14)

$A_V = [(\mu R_L) / (\mu+1)]/ [R_L + r_d (\mu+1)]$ (2.15)

A_V is positive . Therefore there is no phase shift between output and input

With condition $R_L >> r_d / (\mu + 1)$,

Eqn 2.15 can be written as

$A_v \approx \mu / (\mu+1) \approx 1$

When $\mu >> 1$.

2.6 Common Gate FET amplifier

The circuit diagram of common gate amplifier is shown in fig.2.13a

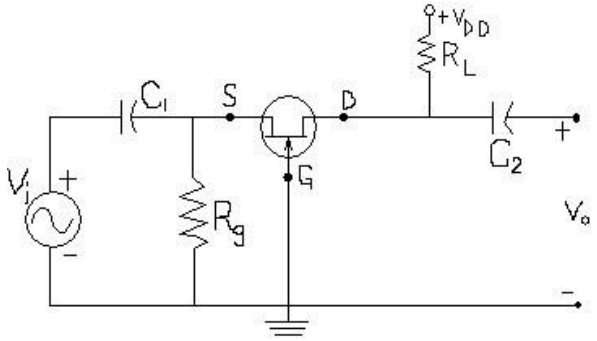


Fig. 2.13a

The A.C. equivalent circuit of fig.4.13a is shown in fig.2.13b .

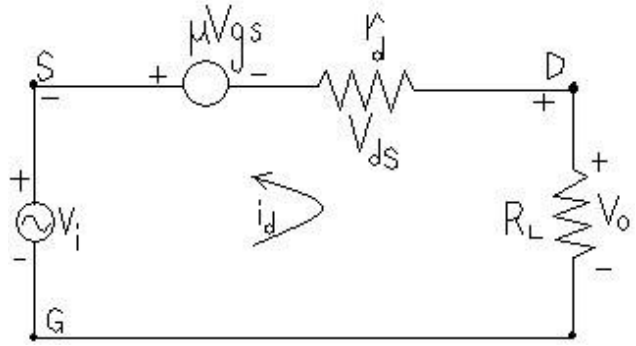


Fig.2.13b

The gain of the common gate amplifier can be expressed as

$$A_v = v_o / v_i = (\mu+1) / [\, 1+ (r_d / R_L)]$$

2.7 MOSFET

There are two types of MOSFET:

a) Enhancement type(E MOSFET)- n channel and p channel

b)Depletion type(D MOSFET) - n channel and p channel

2.7.3 N channel enhancement MOSFET

The structure of n channel enhancement MOSFET is shown in fig2.14 .Two heavily doped n^+ regions (source and drain) are diffused into a lightly doped p type semiconductor bar called as substrate. A thin insulation layer is grown over the structure and then metallic contacts are made from source and drain. Gate metallic contact is grown over the oxide.

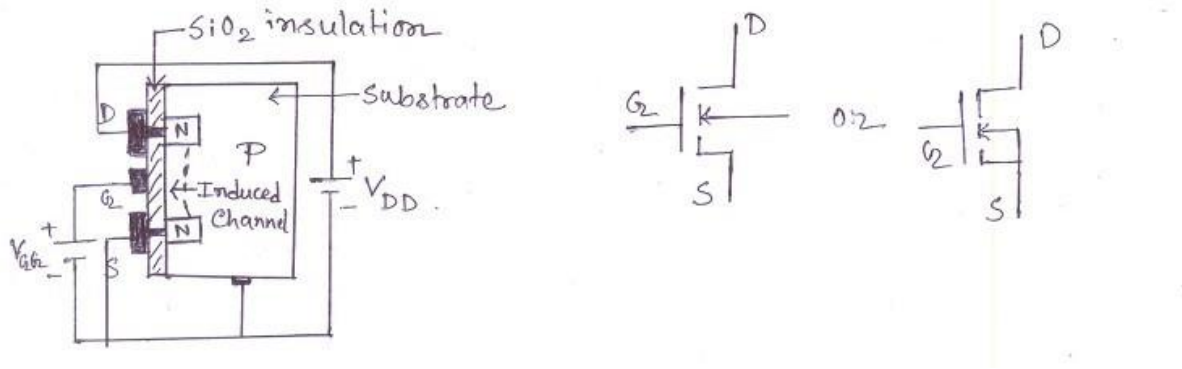


Fig 2.14: N channel enhancement MOSFET and its symbol

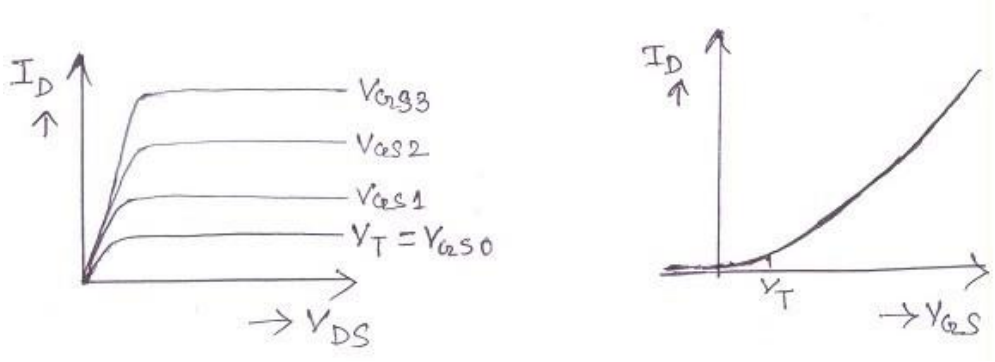
For n channel enhancement MOSFET the drain and gate is positive, source and substrate is grounded. V_{DD} and V_{GG} are the drain and gate supply voltages respectively. There is no permanent channel in this type of MOSFET. As the gate is positive, negative charges those are minority carriers in p substrate, are induced in the region between source and drain and inversion layer is formed. The minimum value of gate to source voltage V_{GS} which forms the inversion layer is called the threshold voltage $V_{T.}$ So, the n channel is built up between source and drain.

2.7.4 Drain Characteristics

It is the I_D vs V_{DS} characteristics curve. As the drain is positive with respect to source, the electrons flow from source to drain and drain current I_D increases linearly as shown in fig2.15(a). Again, p substrate is grounded and n type drain is positive. So, p-n junction is reverse biased and depletion layer is formed. If drain to source voltage V_{DS} is more positive, the depletion region is widened and it blocks the channel, so pinch off occurs. Then I_D gets saturated as shown in fig2.15 (a).By changing the V_{GS} a family of curves are formed.

2.7.5 Transfer Characteristics:

It is the I_D vs V_{GS} characteristics curve. Here, if V_{GS} is increased, the saturation occurs at higher values of I_D ,so a nonlinear variation of I_D with V_{GS} as shown in fig 2.15(b).

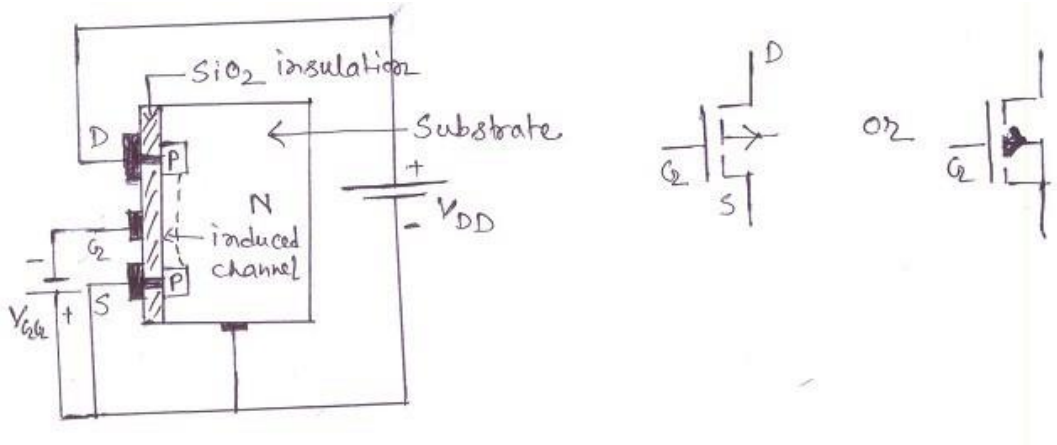


(a) (b)

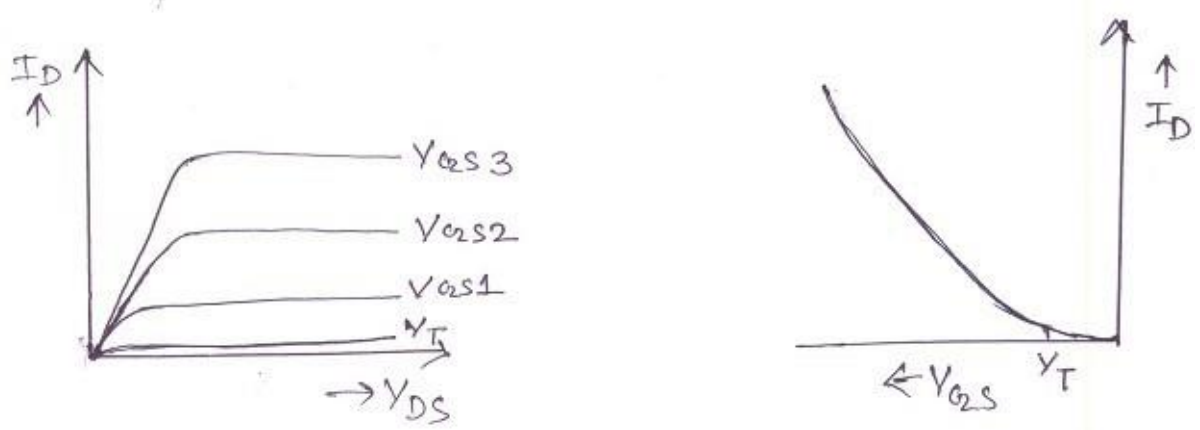
Fig 2.15 (a) Drain Characteristics and (b) Transfer Characteristics of n channel enhancement MOSFET

2.7.6 P channel enhancement MOSFET

Here drain and source is p type and substrate is n type. As gate is negative positive charges accumulated in between source and drain, so p channel is formed as in fig 2.16(a).The characteristics curve formation shown in fig 2.16(c) & (d) is same like n channel enhancement MOSFET.



(a) (b)



(c) (d)

Fig 2.16 : p channel enhancement MOSFET (a) schematic,(b) symbol (c)drain characteristics,(d)transfer characteristics

2.7.7 N channel depletion MOSFET:

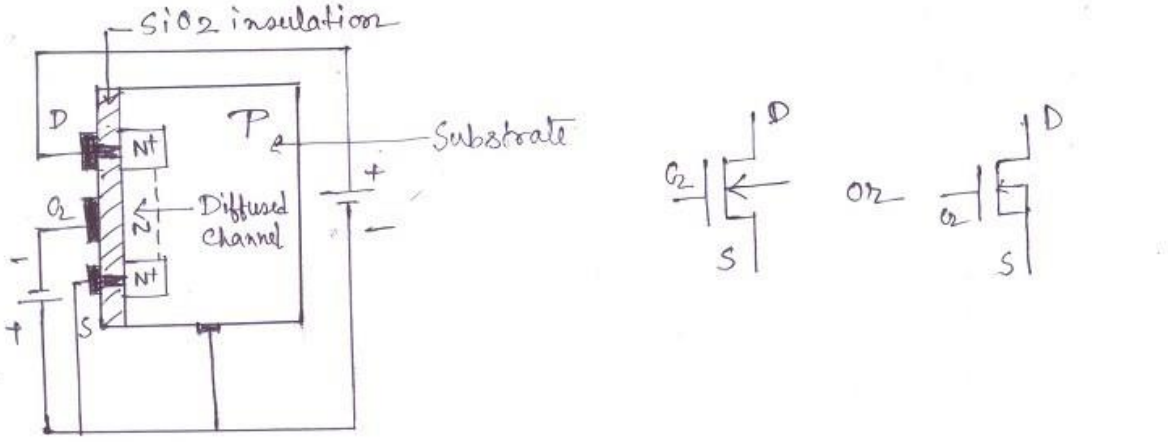


Fig2.17 : N channel depletion MOSFET and its symbol

In n channel depletion MOSFET a n channel is diffused between n+ type source and drain in a p type substrate by doping. Here the doping concentration is much less than source and drain.

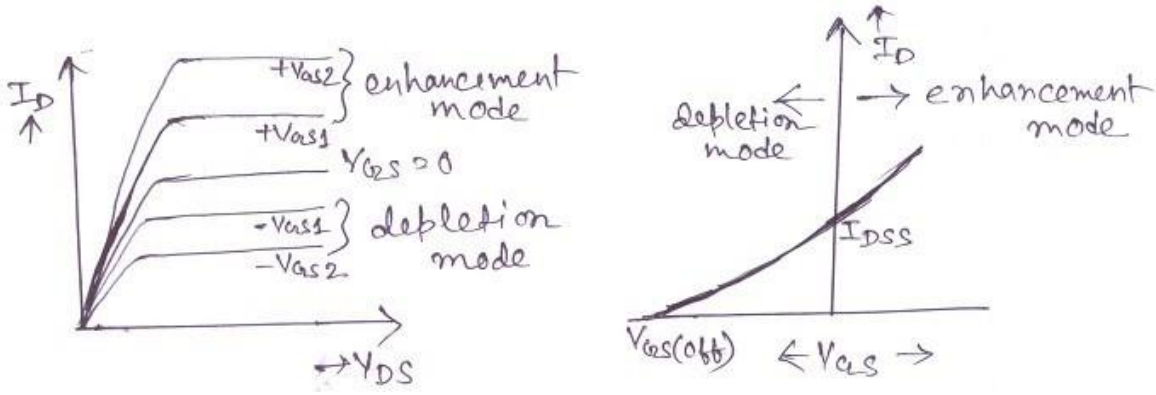
2.7.8 Drain Characteristics:

If V_{DS} is positive and V_{GS} is zero, then electrons flow from source to drain. Drain current I_D linearly increases. If V_{DS} more positive, the depletion region at p-n junction widens and pinch off occurs, then I_D gets saturated. If V_{DS} is positive and V_{GS} is negative, as the gate is negative, positive charges are induced in n channel. So, electron-hole recombination takes place and the depletion of free carriers in the channel occurs. As the no. of free carriers decreases, so I_D decreases and saturation occurs earlier. This is called depletion mode operation. If V_{DS} is positive and V_{GS} is positive, negative charges are induced in n channel. So the no. of free carriers increases and I_D increases and saturation occurs later. This is called enhancement mode operation. The drain characteristic is shown in fig 2.17 (a).

2.7.9 Transfer Characteristics:

In depletion mode I_D becomes zero when gate voltage is $V_{GS(off)}$ and in enhancement mode I_D increases rapidly with V_{GS}.It is shown in fig 2.17 (b).

$I_D = I_{Dss} [1- V_{GS}/ V_{GS(off)}]^2$, I_{Dss} is the saturation drain current

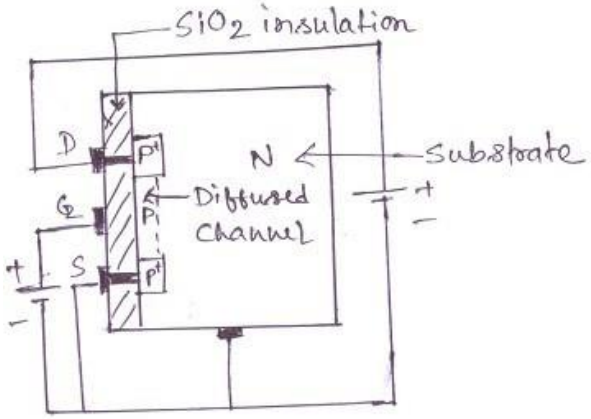


(a) (b)

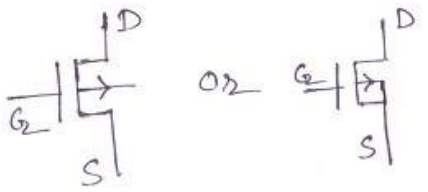
Fig2.17 (a) Drain Characteristics and (b)Transfer Characteristics of n channel depletion MOSFET

2.7.10 P channel depletion MOSFET

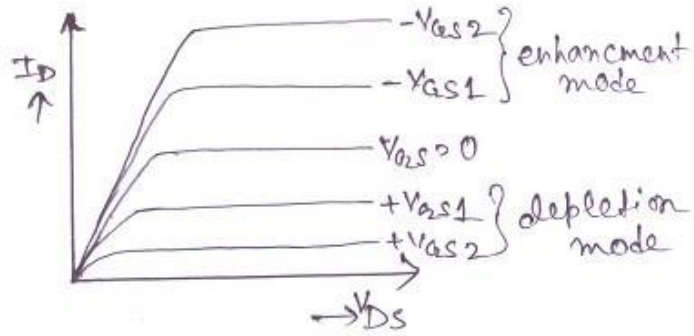
Here drain and source is p type and substrate is n type. p channel is doped between source and drain as in fig2.18(a).The characteristics curve formation shown in fig2.18(c) & (d) is same like n channel depletion MOSFET.



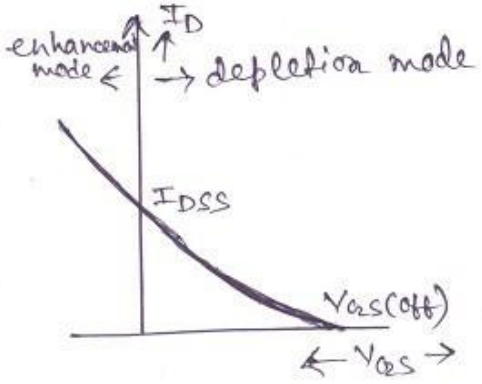
(a)



(b)



(c)



(d)

Fig 2.18 :p channel depletion MOSFET (a) schematic,(b) symbol,(c)drain characteristics,(d) transfer characteristics

2.8 Example with hints

Example : 4.1. When drain-source voltage of a JFET is changed by 1.5 volts, the change in drain current is of 120 μA, the gate-source voltage remaining un-changed. Determine the ac drain resistence of the JFET.

Hints : $\Delta V_{DS} = 1.5V$, $\Delta I_D = 120 \times 10^{-6} A$

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} = 12.5 k\Omega$$

Example 4.2 prove that $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_p}\right)$

$$= \frac{2}{|V_p|}\left(I_{DSS} I_{DS}\right)^{\frac{1}{2}}$$

Hints :

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$g_m = \frac{\partial i_D}{\partial v_{GS}}\Big|_{V_{DS}}$$

Example 4.3 For an n-channel JFET

$I_{DSS} = 8.7 mA$; $V_p = -3V$; $V_{GS} = -1V$

Find the values (i) I_D (ii) g_{mo} (iii) g_m

Hints. $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

$$g_{mo} = -\frac{2 I_{DSS}}{V_p}, \quad g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_p}\right)$$

Example 4.4 A FET Amplifier operating in common source mode. It uses load resistance of 300 kΩ, a.c. drain resistance of 105 kΩ and the transconductance of 0.6 mA/V. calculate voltage gain & output resistance of the amplifier.

Hints:

$$A_V = -\frac{\mu R_L}{r_d + R_L}$$

Example 4.5 An n-channel JFET has $I_{DSS} = 10\,mA$, $V_p = -4\,V$. Determine the minimum value of V_{DS} for pinch-off region & drain current I_D for $V_{GS} = -2\,V$ in pinch-off region.

Hints:

- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$
- $V_{DS(min)} = V_p$

2.9 Sample Questions

1. Choose correct alternative

i) Which one is unipolar device?
(a) n-p-n transistor (b) p-n-p transistor (c) p-n diode (d) FET

ii) The voltage gain of common drain amplifier is closed to
(a) 10 (b) 100 (c) unity (d) none

iii) Pinch-off phenomenon occurs in FET near to
(a) source terminal (b) drain terminals (c) gate terminal (d) center of the channel

iv) Type of source, drain and substrate in an enhancement NMOS respectively as
(a) n , n ,p (b) p ,p, p (c) n ,n, n (d) p , n, p

v) FET can be used as a voltage variable resistor in
(a) saturation region (b) linear region (c)cut-off region (d) break-down region

2. Give different classification of FET

3. Explain the construction of n-channel JFET

4. Explain the principle of operation of n-channel JFET

5. What do you mean by pinch-off Voltage?

6. Find out relationship among FET parameters.

7. Explain Common source amplifier circuit and derive its voltage gain

8. Prove that voltage gain of common drain amplifier is approximately equal to unity

9. What do you mean by threshold voltage?

10. Explain the construction and operation of n-channel E-MOSFET

11. (a) Followings readings are obtained experimentally from a JFET. Determine drain resistance, trans-conductance and amplification factor of the JFET.

V_{DS} (Volt)	5	12	12
V_{GS} (Volt)	0	0	-0.25
I_{DS} (mA)	8	8.2	7.5

12. Write short notes on DEMOSFET

13. A FET amplifier in the common source configuration uses a load resistance of 150KΩ. The drain resistance of the device is 100KΩ and the transconductance is 0.5mA/V. What is the voltage gain of the amplifier?

Assignment

1. Make a difference between BJT and FET
2. What are difference between E-MOSFET and DE-MOSFET?
3. How FET can be used as an voltage variable resistor?
4. Explain the drain characteristics of n-channel JFET.
5. How transfer characteristics of JFET can be obtained from drain characteristics?

Module-III: Feedback and Operational Amplifier 10 L

3.1 Introduction to Feedback

- Feedback is the process in which some fraction of the output is returned back to the input. Using feedback the performance of an amplifier can be changed
- To design amplifier and oscillator feedback paly major role
- In the following section we will discuss the about features of feedback and its effect on amplifier performance parameters.

3.2 Concept of feedback with block diagram, positive and negative feedback, gain with feedback

- There are two types of feedback-Positive feedback & Negative feedback
- In case of positive feedback output signal is in phase with the input signal and the amplitude of the input signal, increases ,resulting the increase in the gain
- The positive feedback is also known as regenerative feedback
- Oscillator, multi vibrator are designed using positive feedback etc.
- In case of negative feedback gain of the amplifier reduces
- Negative feedback also known as degenerative feedback
- Phase difference between output and input for negative feedback is 180^0.

Followings advantages are observed from negative feedback

(i) Gain is stabilized

(ii) Distortion is reduced

(iii) Noise is reduced.

(iii) Based on feedback topology Input impedance is increased or decreased

.

(iv) Based on feedback topology Output impedance can be increased and decreased.

(v) Increase in the range of uniform amplification.

(vi) Band width increases

3.3 Block diagram of feedback amplifier

The general block diagram of feedback amplifier is shown in fig3.1

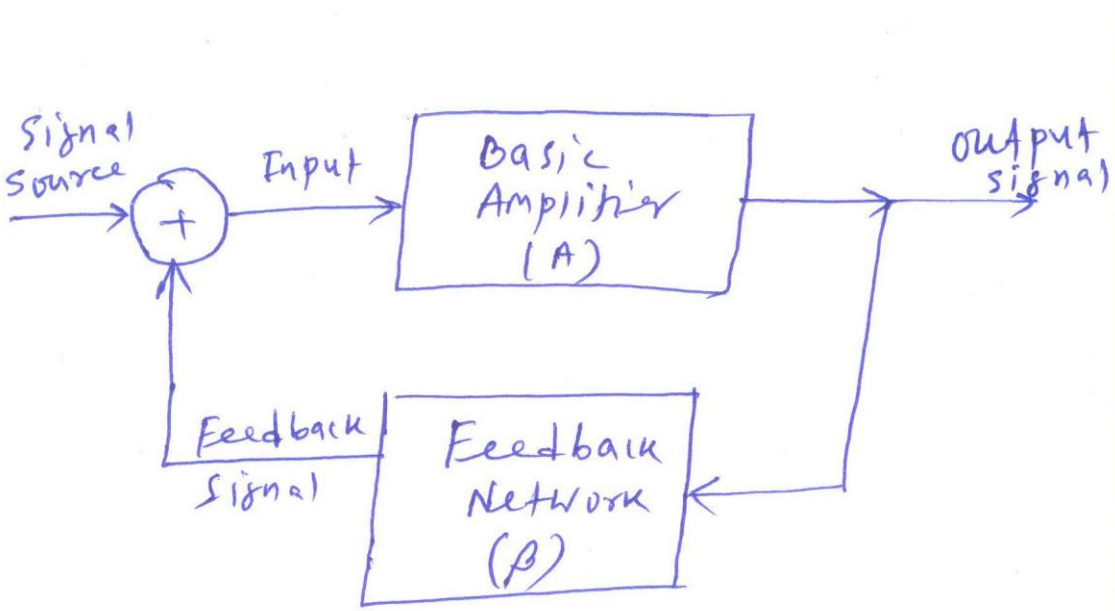


Fig. 3.1. Block schematic of feedback amplifier

The gain with feedback can be expressed as

$$Af = \frac{A}{1+A\beta} \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.1)$$

Please note

i) For positive feedback Af >A

ii) For negative feedback Af <A

3.4 Feedback topologies, effect of feedback on input and output impedance, distortion

3.4.1 Feedback topologies

3.4.1.1 There are four different types of feedback topologies depending on the input signal (voltage or current) to be amplified and form of the output signal (voltage or current)

3.4.1.2 Alternately depending on sampling signal and mixing signal

3.4.1.3 Topologies are (i) Voltage-Series feedback (ii) Current Series Feedback (iii) Voltage shunt feedback (iv) Current shunt feedback

3.4.1.4 Usually the 1st term in feedback topology indicates the sampling term and 2nd term indicates mixing term.

The different types of feedback topology is described below-

a) **Voltage-series feedback (voltage-sampling and series mixing topology)**

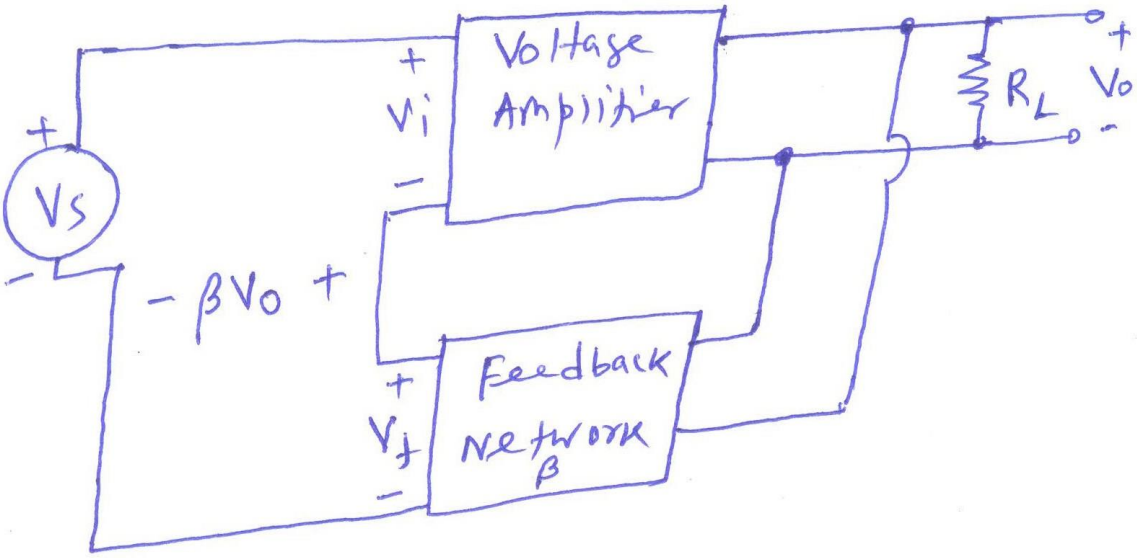


Fig.3.2 Configuration of voltage series feedback topology

- Here both the output signal and the feedback signal are voltage signal and the voltage is feedback to the input in series
- Therefore, it is also called as shunt-series feedback.
- It provides high input impedance and low output impedance
- This type of feedback topology is used in voltage amplifiers

b) **Current series feedback (Series sampling – series mixing)**

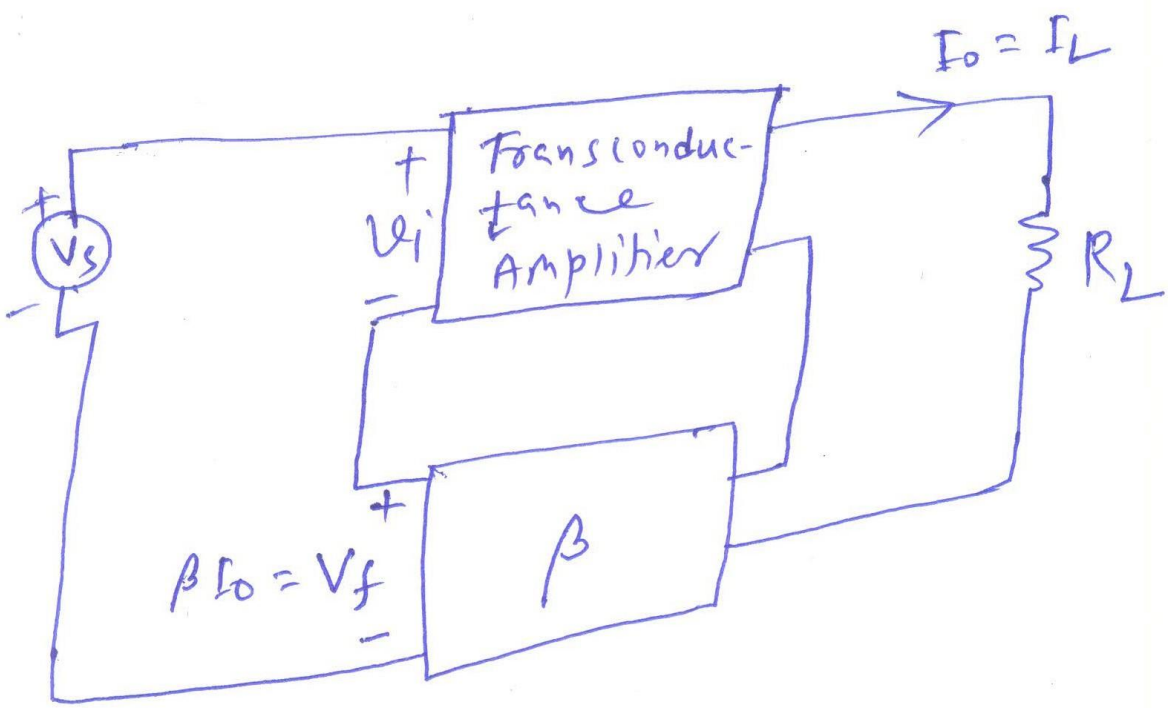


Fig 3.3 Current series feedback configuration

3.4.1.5 Here, the output signal is current signal, but the feedback signal is voltage signal and the voltage is feedback in series to the input

3.4.1.6 Therefore, it is also called as series-series feedback

3.4.1.7 This employed high input and output impedance

3.4.1.8 This type of feedback topology is used in trans-conductance amplifiers

c) **Voltage shunt (Shunt sampling –shunt mixing)**

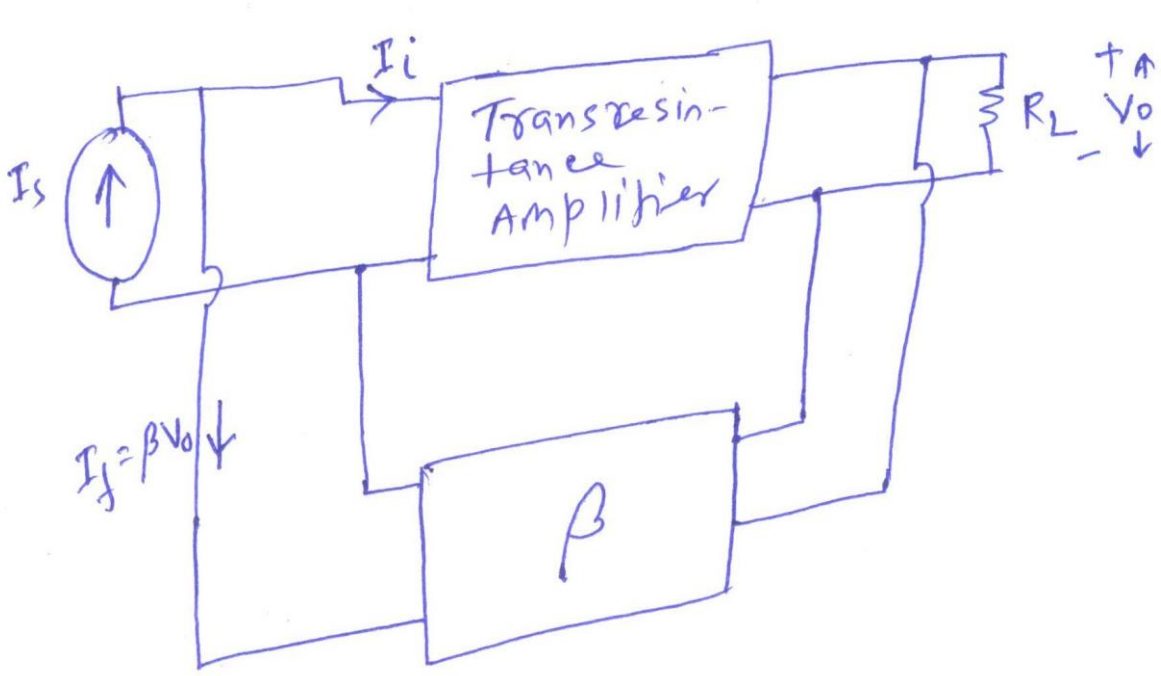


Fig. 3.4 Voltage shunt feedback configuration

3.4.1.9 Here the output signal is voltage signal, but the feedback signal is current signal
3.4.1.10 Therefore, it is also called as shunt-shunt feedback
3.4.1.11 This topology provides low output impedance and low input impedance
3.4.1.12 This type of feedback topology is used in trans resistance amplifier.

d) **Current shunt (Current sampling – shunt mixing)**

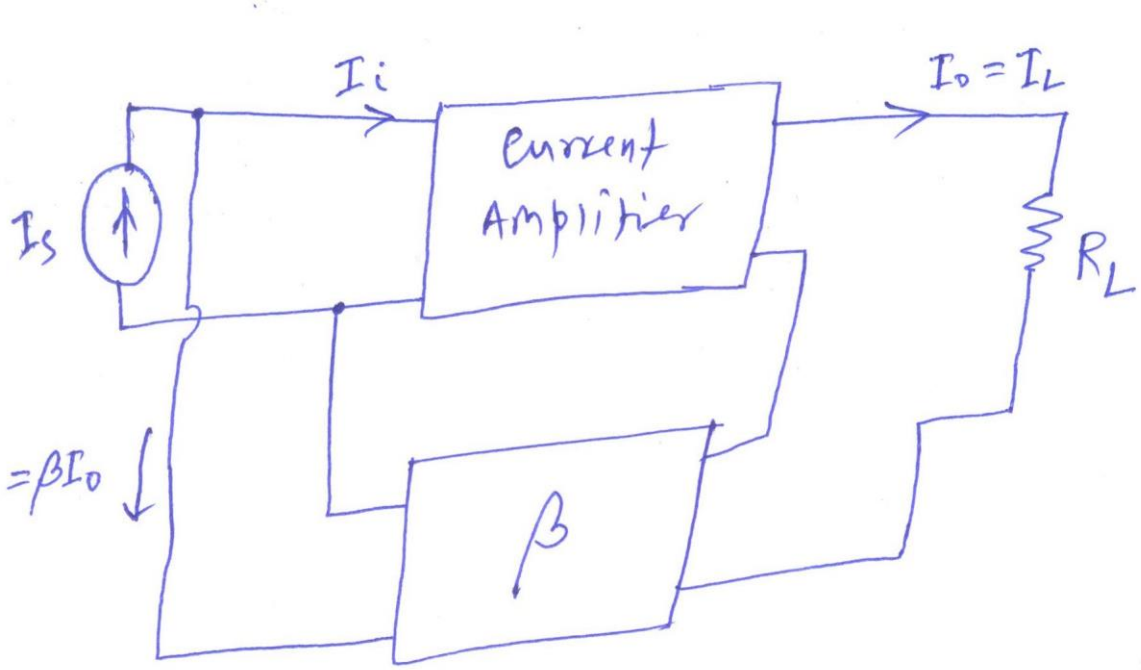


Fig. 3.5 Current shunt feedback configuration

3.4.1.13 Here both the output signal and the feedback signal are current signal
3.4.1.14 The current is feedback in shunt to the input
3.4.1.15 Therefore, it is also called as series-shunt feedback
3.4.1.16 It provides high input and low output impedance
3.4.1.17 This type of feedback topology is used in current amplifiers.

3.4.2 Effect of feedback on input and output impedance

Calculation of Input Impedance:

3.4.2.1 Series mixing feedback circuit

In the voltage series feedback circuit of Fig 3.2 the input impedance of the amplifier without feedback is given by –

$Z_i = \frac{V_i}{I_s}$, Where V_i is the voltage preceding the basic amplifier

The input impedance with feedback is given by-

$$Z_{if} = \frac{V_s}{I_s}$$

or, $Z_{if} = \frac{V_i + V_f}{I_s} = \frac{V_i + \beta V_0}{I_s}$

or, $Z_{if} = \frac{V_i + A\beta V_i}{I_s} = \frac{V_i(1+A\beta)}{I_s}$

or, $Z_{if} = Z_i\ (1 + A\ \beta)$

For negative feedback (1+Aβ)> 1, therefore it indicates that the input impedance of the amplifier increases when the feedback signal is added in series with the externally applied signal.

Shunt mixing feedback circuit

The current gain of the amplifier of Fig.3.5 is represented by A.

Where, $A = I_0 / I_i$, where I_i is the current towards the basic amplifier

Input impedance of the amplifier without feedback is given by-

$Z_i = V_s/I_i$

The input impedance of the amplifier with feedback.

$Z_{if} = V_s/I_s$

Now, $I_s = I_i + I_f$

$= I_i + \beta I_0$

$= I_i + A\beta I_i = I_i(1+A\beta)$

So, $Z_{if} = \frac{V_S}{I_i(1+A\beta)} = \frac{Z_i}{(1+A\beta)}$

Since, (1+Aβ)> 1 for negative feedback, so the input impedance of the amplifier decreases with shunt connection.

Output Impedance:

3.4.2.2 Output impedance for shunt sampling feedback topology cab be expressed as

$$Z_{of} = \frac{V}{I_s} = \frac{Z_0}{(1+A\beta)}$$

For negative feedback $(1 + A\ \beta) > 1$. Therefore Z_{of} decreases

3.4.2.3 Output impedance for Series sampling feedback circuit is given as

$$Z_{of} = \frac{V}{I_1}$$

$$= \frac{V}{I(1 + A\beta)}$$

$$= Z_0 (1 + A\beta)$$

Since, $(1 + A\beta) > 1$, So, Z_{of} increases for connecting the feedback network in series with output.

3.4.2.4 Effect on phase distortion:

Due to negative feedback the phase distortion is reduced.

3.4.2.5 Feedback Effect on noise :

Due to negative feedback noise will reduce

1.5 Concept of oscillation and Barkhausen criterion

- Oscillator is an electronic circuit which can generate periodic signal at its output with - out application of alternating signal at input
- In this context generator is not an oscillator
- Output of oscillator may be sinusoidal or non-sinusoidal as shown in the fig 3.6

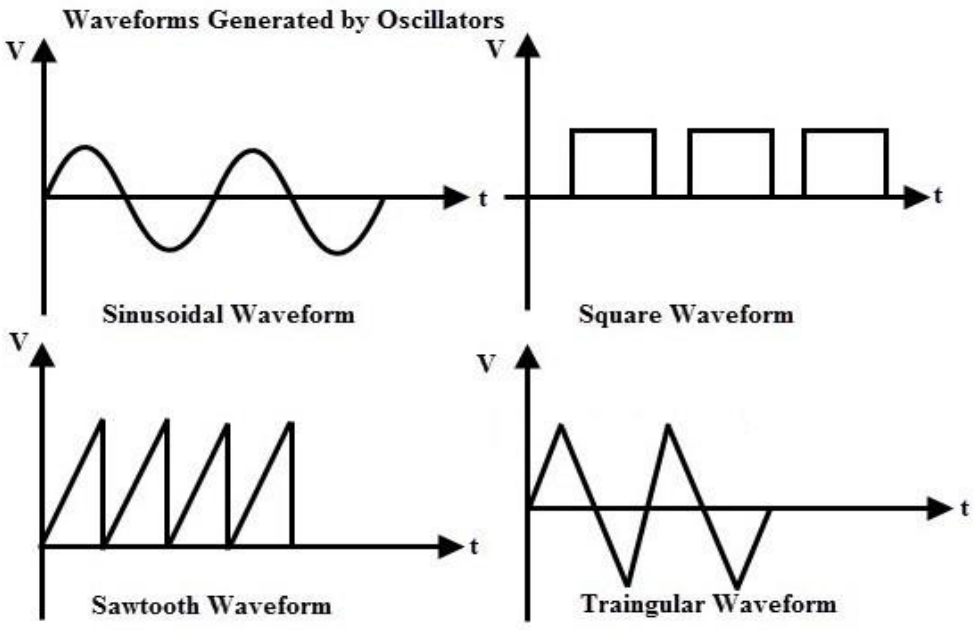


Fig. 3.6 Oscillating waveform

Fig. 3.7 shows the difference between amplifier and oscillator

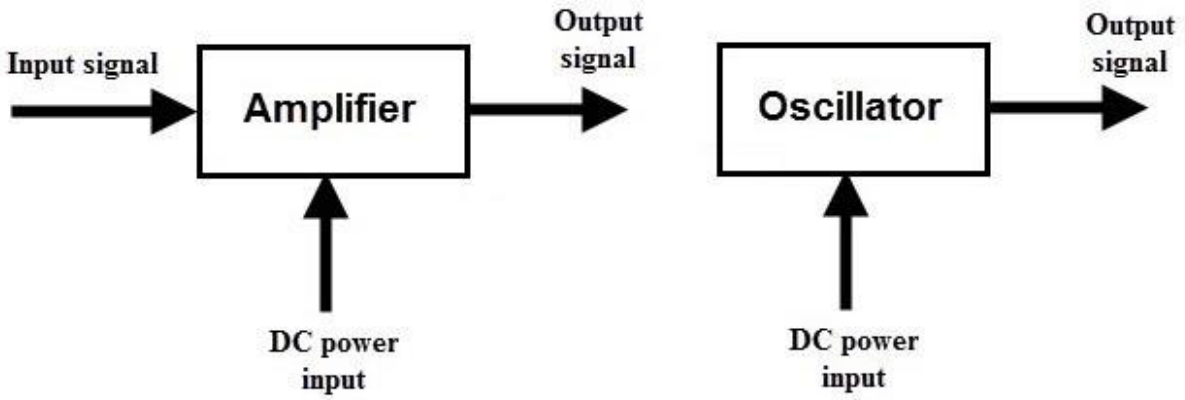


Fig.3.7 : Difference between amplifier and oscillator

Barkhausen Criterion or Conditions for Oscillation

Followings are the Barkhausen criterion for oscillation

1. The closed loop gain must be unity

2. Phase shift around the loop by 0^0 or integer multiple of 360^0

1.6 Operational Amplifier (Op-Amp)

3.6.1 Introduction

- Operational amplifier is a high gain direct coupled amplifier used for some mathematical operation like addition ,subtraction , multiplication ,division e.t.c.
- As it performs mathematical operations hence the name operational amplifier .
- In general op-amps are available in the market in the form of integrated circuit (IC) .
- Example of one commonly used op-amp is IC 741 .

3.6.2 Operational amplifier – electrical equivalent circuit ,ideal characteristics , Non ideal characteristics of op-amp – offset voltages ,bias current , offset current Slew rate , CMRR and bandwidth .

Familiarity with IC741: Pin diagram of IC 741 is shown in Fig.3.8

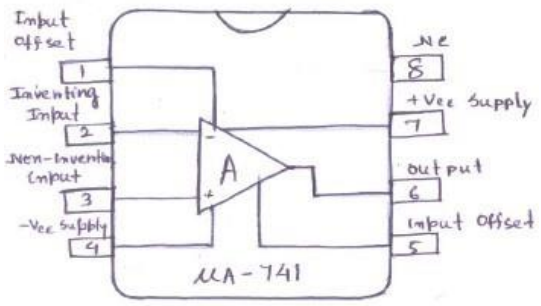


Fig.3.8 Op-amp µA-741 Pin configuration

Electrical equivalent circuit of Op-Amp: The electrical equivalent circuit of op-amp shown in fig. 3.9

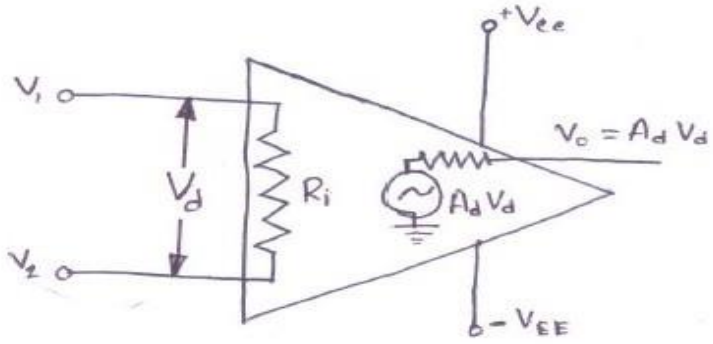


Fig.3.9 Electrical equivalent circuit of an OPAMP

3.6.2.1 v_1 and v_2 are the input signal

3.6.2.2 Input impedance has been denoted by R_i

3.6.2.3 In the output side $A_d V_d$ is an equivalent Thevenin voltage source and R_O is the output impedance

3.6.2.4 Output voltage V_O is Output voltage can be expressed as

$$\mathbf{V_O = A_d (v_1 - v_2) = A_d V_d.}$$

Ideal characteristics: An ideal OPAMP exhibits the following electrical characteristic.

a) Infinite open loop voltage gain
b) Infinite input resistance
c) Zero output resistance
d) Input and output off-set voltage is zero
e) Infinite bandwidth
f) Infinite CMRR
g) Infinite slew rate

Voltage Transfer Characteristics of OP-AMP

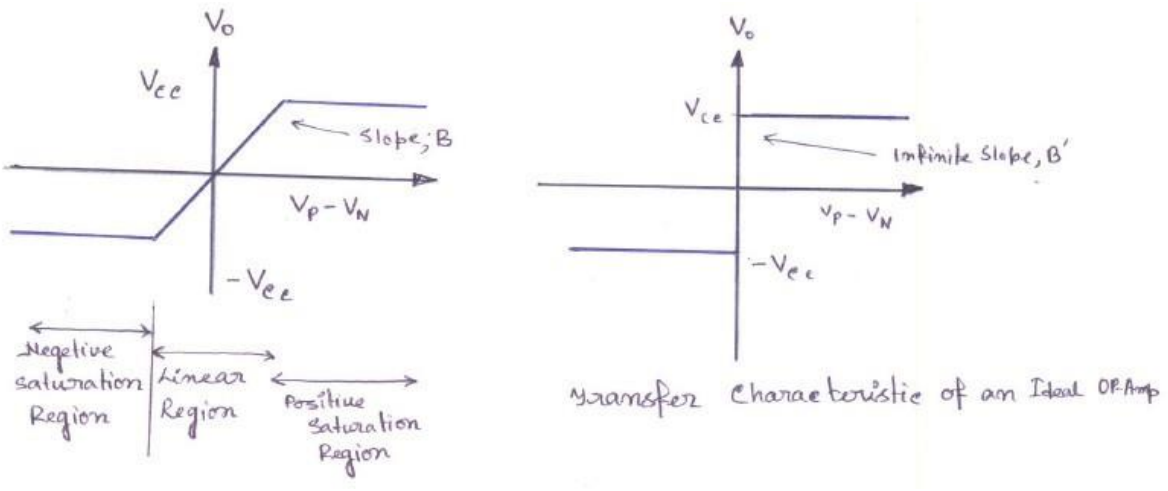


Fig. 3.10 Voltage transfer characteristic of practical op amp and ideal transfer characteristic of an op amp with an infinite gain

Non ideal characteristics of op-amp

Non ideal characteristics of an op-amp are explained below

Output offset Voltage

For an ideal op-amp if input terminals are grounded then output would be at zero potential. However for non-ideal op-amp although input terminals are grounded some voltage appear at output terminal. This voltage is known as output offset voltage.

Input offset voltage

It is the amount of voltage that is to be applied at input terminals to nullify the output offset voltage.

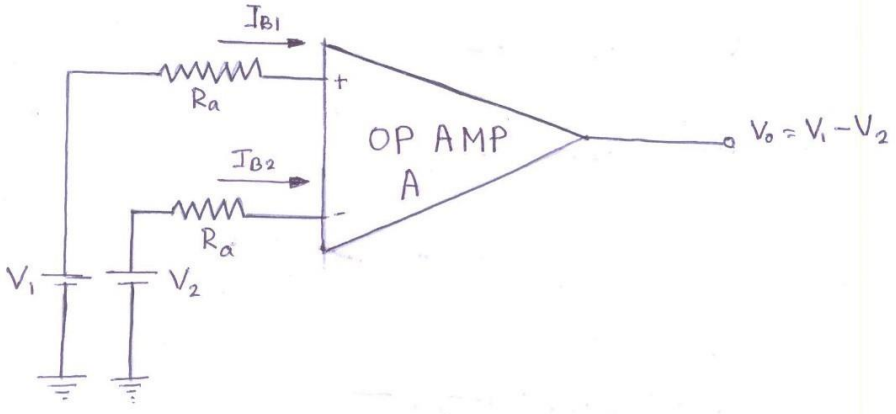


Fig.3.10 Operation showing effect of input offset voltage

Input offset Current

The input offset current is defined as the difference between the currents drawn by inverting and non-inverting terminals at balanced condition. It can be expressed as

$$I_{io} = |I_{B1} - I_{B2}|$$

I_{io} is of the order of nano ampere

The input bias current I_B is the average of the current entering into the inverting and non-inverting terminals for biasing condition

$$i_B = \frac{i_{B1} + i_{B2}}{2}$$

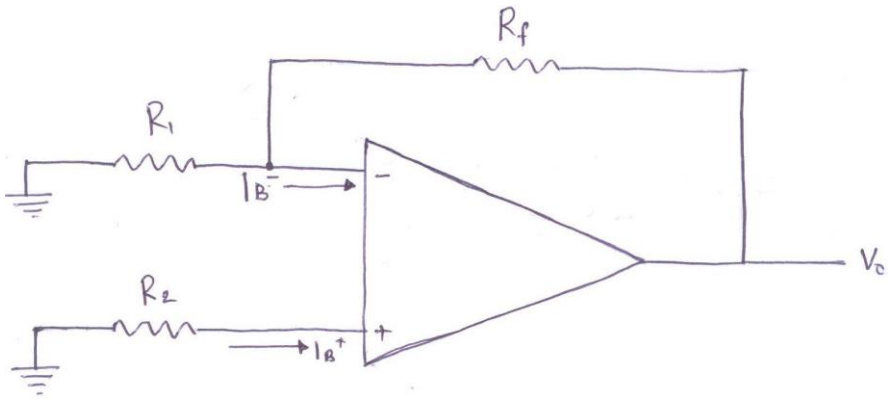


Fig.3.11 Connection diagram to realize bias current of Op-amp.

Slew rate: Slew rate can be expressed as the rate of change of output voltage . It signifies how fast output of an op-amp responding .Slew rate is usually measured in the unit (**Volt/µSec.**) and can be expressed as

$$SR = \frac{\Delta V_o}{\Delta t} \quad V/\mu s$$

Slew rate is very important parameter used to the maximum operating frequency of the op-amp.

CMRR (Common-mode rejection ratio)

- An ideal op-amp can amplify the difference between two input signals at its input
- However in addition with difference mode signal a practical op-amp amplify signal which are common to both the terminals of inputs of op-amp
- This means a practical op-amp has both difference mode gain and common mode gain. Common mode rejection ratio can be defined as the ratio of difference mode gain(A_d) to common mode gain(A_c) .

$$CMRR = \frac{A_d}{A_c}$$

- The value of CMRR can also be expressed in logarithmic terms as

$$CMRR(log) = 20 \log_{10} \frac{A_d}{A_c} \ (\text{In dB})$$

- We can express the output voltage in terms of the value of CMRR as follows:

$$V_o = A_d V_d \left(1 + \frac{1}{CMRR} \frac{V_c}{V_d}\right)$$

- For an ideal operational amplifier CMRR should be infinite ,i.e. common mode gain should be zero
- Therefore CMRR signifies that: how much op-amp is capable to reject common mode signal.

Bandwidth

- We know gain-band width product of an amplifier is constant
- Although bandwidth for an ideal op-amp is infinite practically it has finite band width
- In open loop mode op-amp band width is very low it around 100Hz or less
- But bandwidth can be changed employing feedback
- Bandwidth is measured from gain versus frequency response curve of an op-amp considering -3dB points

3.6.3 Configuration of inverting and non-inverting amplifier using Op-amp, closed loop voltage gain of inverting and non-inverting amplifier

Configuration of inverting and non-inverting amplifier using Op-amp

3.6.3.1 There are two basic ways to configure the voltage feedback op amp as an amplifier

3.6.3.2 Figure 5.12 shows what is known as the inverting configuration. With this circuit, the phase difference between input and output is 180^0.

3.6.3.3 The gain of this circuit is determined by the ratio of the resistors used and is given by:

$$A = -\frac{R_{fb}}{R_{in}}$$

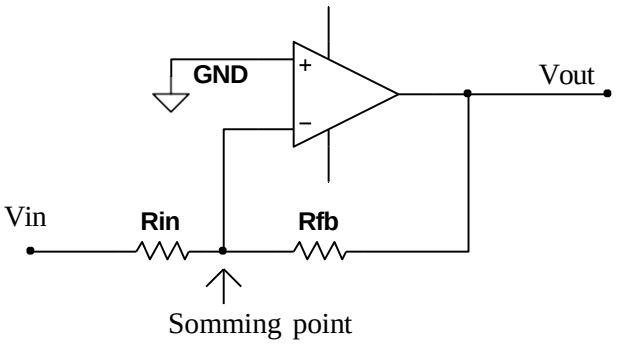


Figure 3.12 Inverting amplifier using op-amp

3.6.3.4 Figure 5.13 shows what is known as the non-inverting configuration

3.6.3.5 With this circuit the output is in phase with the input

3.6.3.6 The gain of the circuit is also determined by the ratio of the resistors used and is given by:

$$A = 1 + \frac{R_{fb}}{R_{in}}$$

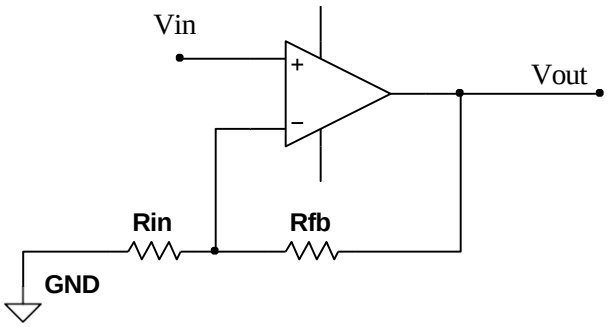


Figure 3.13: Non-inverting Amplifier using op-amp

3.6.3.7 An analogy to understand the amplifier with feedback using pivot-lever system

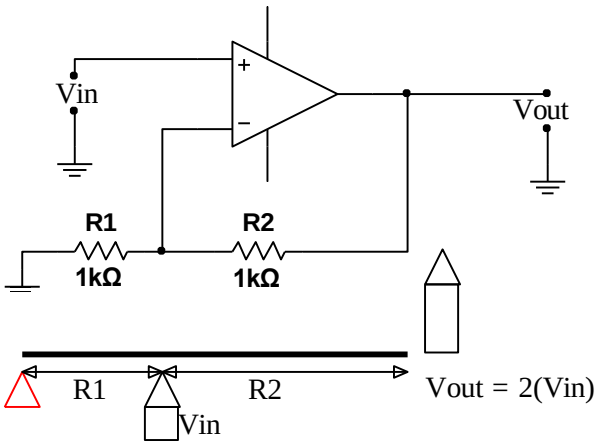


Fig. 3.14

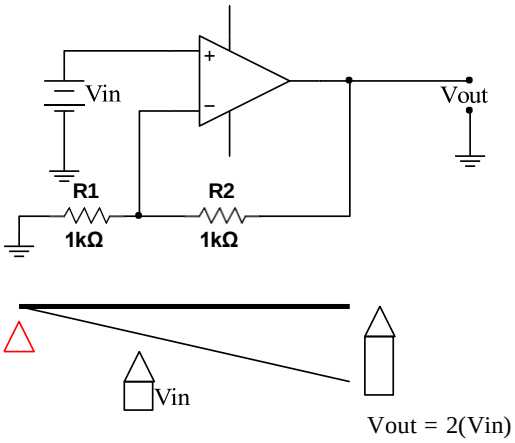


Fig.3.15

3.6.4 Applications op-amp – summing amplifier, differential amplifier, voltage follower, basic differentiator and integrator

Inverting summer

3.6.4.1 The configuration as shown in following Fig.3.16 can be used as a summing amplifier. Where three input voltages are V_a, V_b & V_c. R_f is feedback resistor and the input resistors are R_a, R_b, R_c.

For an ideal opamp $V_1=V_2=0$, from virtual ground concept . so applying KCL at node V_2 we can write

$$I_1+ i_2+i_3=i_f$$

$$(V_a/R_a)+(V_b/R_b)+(V_c/R_c)= -V_0/R_f$$

$$V_0= - R_f (V_a/R_a+V_b/R_b+V_c/R_c)$$

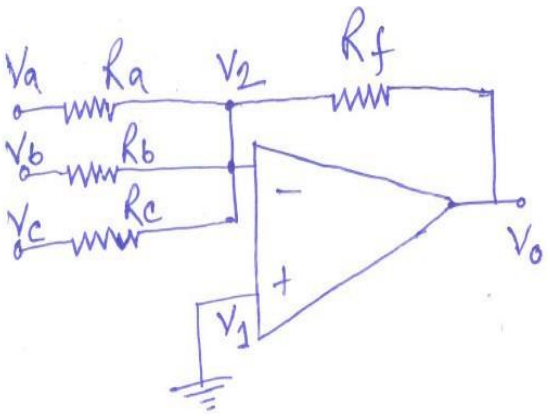


Fig.3.16 Inverting Summer Circuit

If in the above equation $R_a=R_b=R_c$ then above equation reduced to

$$V_0= - (R_f /R)(V_a+V_b+V_c)$$

3.6.4.2 Therefore the output voltage is equal to the negative sum of all the inputs times the gain of the circuit R_f/R.

3.6.4.3 Hence the circuit is called a summing amplifier

3.6.4.4 In the above expression if $R_f= R$ then the output voltage is equal to the negative sum of all inputs as $V_o= -(V_a+ V_b+ V_c)$ and the circuit is said to be adder in inverting mode .

Non Inverting summer

3.6.4.5 The configuration as shown in following Fig.3.17 can be used as a summing amplifier

3.6.4.6 Where three input voltages are V_a, V_b & V_c. R_f is feedback resistor and the input resistors are R_1 for inverting input terminal and R for non-inverting input terminal.

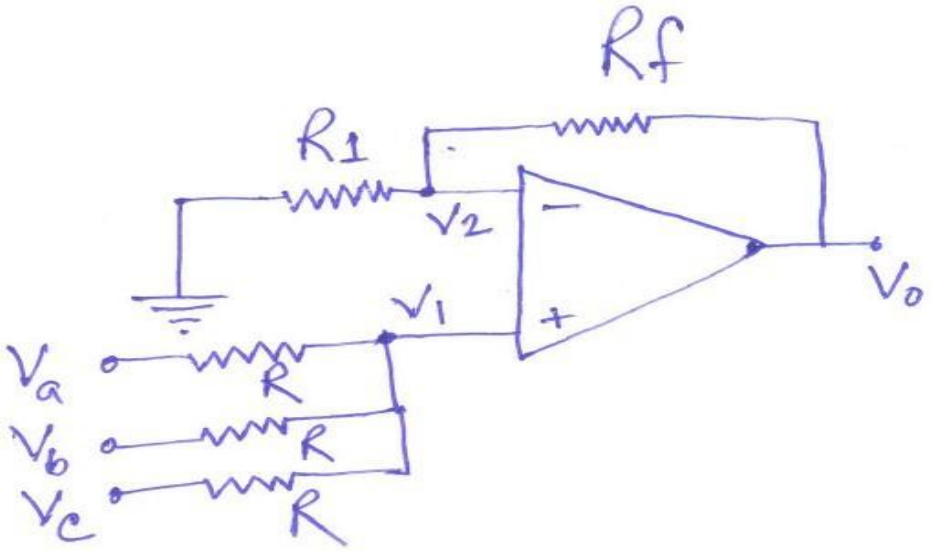


Fig.3.17 Non Inverting Summer Circuit

3.6.4.7 Now for an ideal OP-AMP, $V_1 = V_2$ (Virtual short Concept). The current drawn by OPAMP is zero

3.6.4.8 Thus, applying KCL at V_1 node we

can write $[(V_a-V_1)/R]+[(V_b-V_1)/R]+[(V_c-V_1)/R]=0$

Therefore $V_1=1/3(V_a+V_b+V_c)$

Now $V_o=(1+R_f/R_1)V_1=1/3\ (1+R_f/R_1)(V_a+V_b+V_c)$

If $R_f=2R_1$ Then $V_o=(V_a+V_b+V_c)$.

So output voltage is summation of all input voltages.

Voltage follower

A voltage follower (also called a unity-gain buffer) is an op-amp circuit which has a voltage gain of 1 as shown in Fig.3.18.

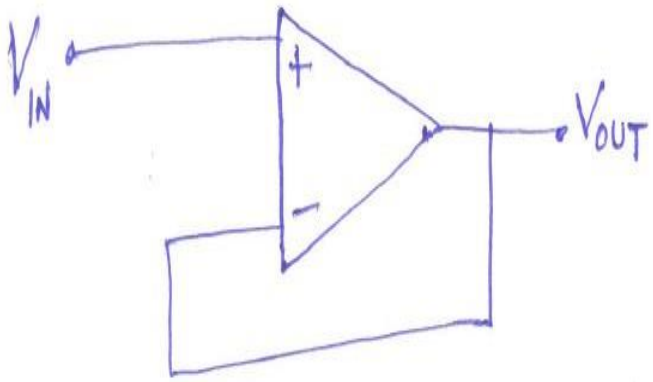


Fig.3.18 Voltage follower circuit

It can be proved that output voltage of the above circuit $V_{OUT} = V_{IN}$, i.e. gain of the circuit is unity

Differential Amplifier

The basic differential amplifier is shown in Fig.3.19

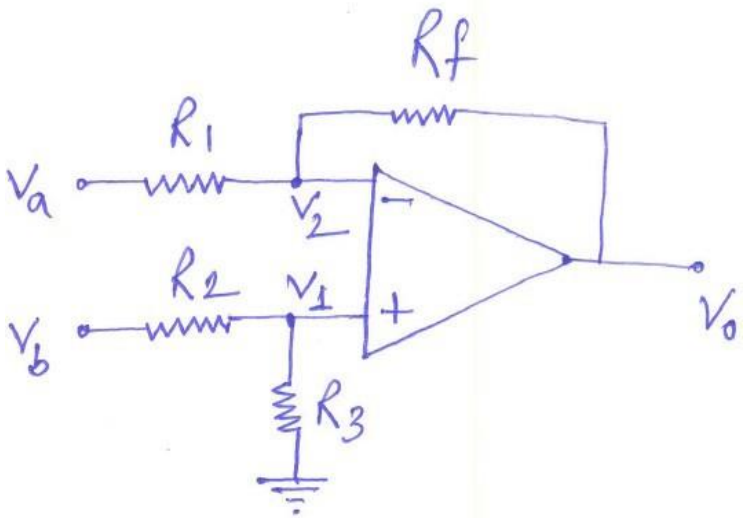


Fig.3.19 Differential Amplifier Circuit

3.6.4.9 Two signal sources are acting at inputs

3.6.4.10 Superposition theorem has been used to find the output voltage. When $V_b = 0$, then the circuit becomes inverting amplifier and the output due to only V_a is $V_{o(a)} = -(R_f / R_1) V_a$

3.6.4.11 Similar way whenever Va = 0, the configuration is a inverting

amplifier. Again, for an ideal OPAMP, $V_1 = V_2$. Voltage at node V_1 can be

calculated as $V_1=(R_3/(R_2+R_3))V_b$

Output voltage due to V_b only can be written as $V_{0(b)} =(1+R_f/R_1)V_1$

Now with condition, if $R_1=R_2$ & $R_3=R_f$ then $V_{0(b)} =(R_f/R_1)V_b$

Output due to V_a only can be written as $V_{0(a)} =(R_f/R_1)V_a$

Therefore total output $V_0=V_{0(a)} + V_{0(b)}$

$$V_0=(R_f/R_1)(V_b-V_a)$$

Now if $R_f=R_1$, then $V_o=(V_b-V_a)$. So this circuit can be used as subtractor circuit.

Differentiator using op-amp

3.6.4.12 A circuit in which the output voltage waveform is the differentiation of input voltage waveform is called differentiator as shown in Fig.3.20

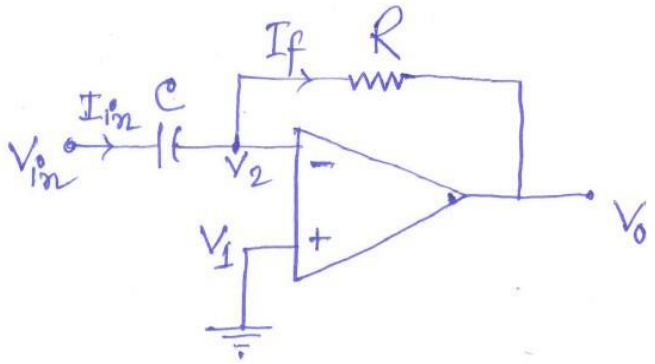


Fig.3.20 Simple differentiator circuit using op-amp

3.6.4.13 The expression for the output voltage can be obtained from the Kirchoff's current equation written at node V_2.

From the circuit of fig.3.20 we can write $I_{in}=I_f$

$= > C [(d/dt)(V_{in}-0)]= (0-V_0)/R$

$= > V_0= - RC [(d/dt)(Vin)]$

The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to RC.

3.6.4.14 If sine wave is applied at the input of differentiator output becomes cosine wave (Fig. 3.21)

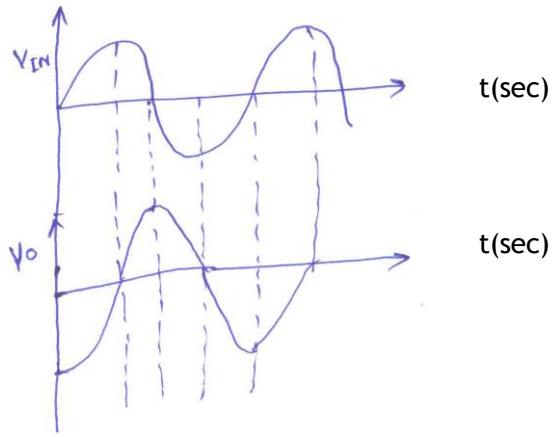


Fig. 3.21

3.6.4.15 If input of differentiator is square wave then output is spike wave as shown in Fig.3.22

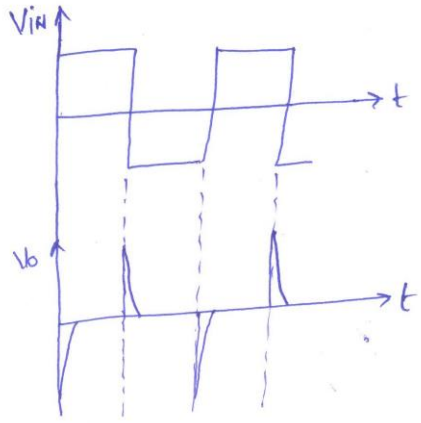


Fig.3.22

Practical differentiator circuit

3.6.4.16 For the basic differentiator circuit as frequency changes, the gain changes and at higher frequencies the circuit becomes unstable

3.6.4.17 Also at high frequency noise and noise gets amplified

3.6.4.18 Both the high frequency noise and problem can be compensated developing practical differentiator circuit by adding, few components. as shown in Fig.3.23.

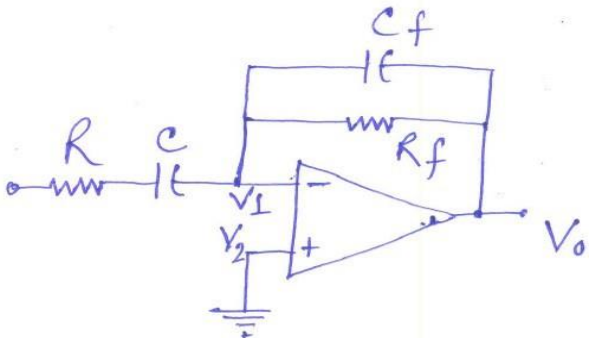


Fig.3.23 Practical differentiator circuit

Basic Integrator circuit

3.6.4.19 A circuit in which the output voltage waveform is integration of input voltage waveform is called an integrator circuit

3.6.4.20 An integrator circuit based on op-amp is shown in Fig.3.24

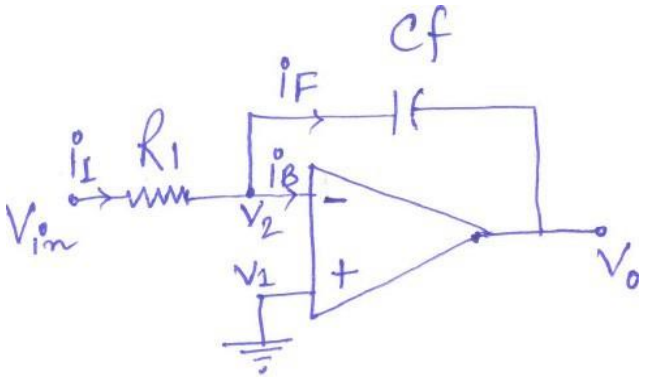


Fig.3.24 Integrator circuit

3.6.4.21 Output voltage of the op-amp integrator can be derived as follows

3.6.4.22 Applying Kirchhoff's current (KCL) at node V_2 we get

$$i_1 = i_F + i_B$$

Since the input resistance of an opamp is very high i_B will be very small and it can be neglected.

Therefore $i_1 = i_F$

Now $i_F = C_f \times (d/dt)\ (V_2 - V_o)$ and $i_1 = (V_{in} - V_2) / R_1$.

So the equation $i_1 = i_F$ can be rewritten as $(V_{in} - V_2) / R_1 = C_f \times (d/dt)(V_2 - Vo)$

As the non-inverting input is connected to ground, V_1 can be taken as 0 Volt and V_2 is zero from virtual ground concept .So we can write

$$\frac{V_{in}}{R_1} = -C_f \frac{d}{dt}(V_o)$$

Integrating the both sides of the above equation with respect to time, we get

$$V_o = -\frac{1}{R_1 C_f} \int V_{in} dt + C$$

The output wave form corresponds to rectangular wave and sine wave is shown in fig.3.25

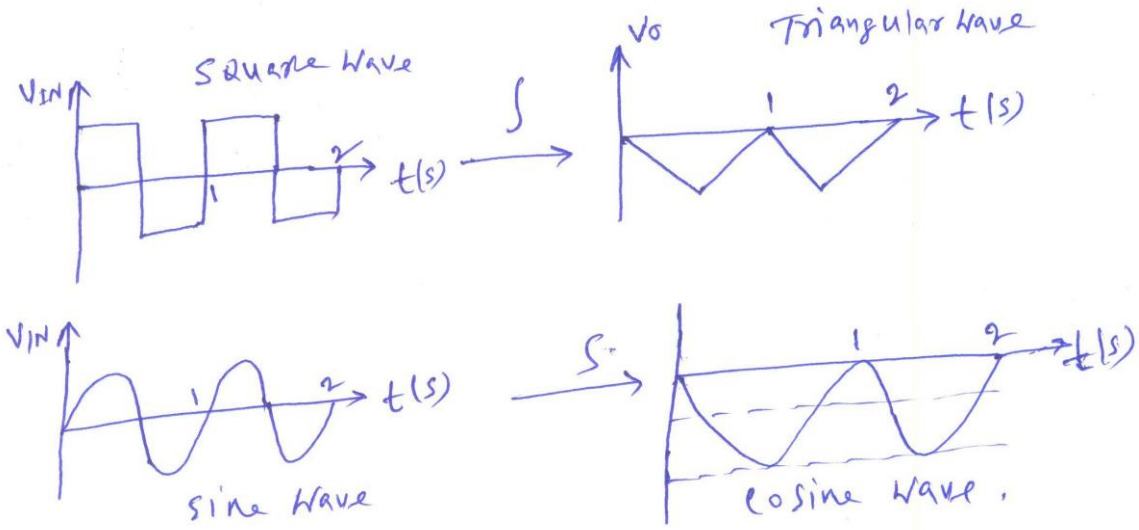


Fig.3.25

3.6.4.23 In the DC condition feedback capacitor C_f offers infinite resistance

3.6.4.24 So signal having very low frequency can't be integrated properly

3.6.4.25 To overcome this problem practical integrator has been developed by connecting one feedback resistance connecting parallel to capacitor as shown in fig.3.26

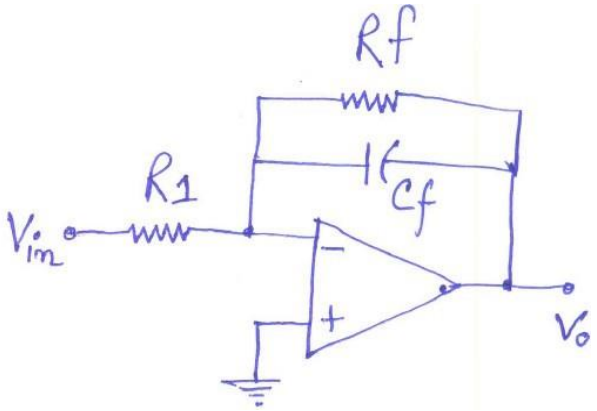


Fig.3.26 Practical op-amp integrator circuit

3.7 Example with hints

Example 5.1 An amplifier with voltage gain of 60 dB uses $\frac{1}{20}$ of its output in negative feedback. Calculate the gain with feedback in dB.

Hints: $A = 60$ dB

$A = 1000$, $\beta = \frac{1}{20}$

$A_f = \frac{A}{1+\beta A}$, $20 \log_{10} A_f$

Example 5.2 Voltage gain of an Amplifier without feedback is 60 dB. It decreases to 40 dB with feedback. Calculate feedback factor

Hints: $A = 60$ dB or 1000

$A_f = 40$ dB or 100

$A_f = \frac{A}{1+\beta A}$, $\beta A = ?$

Example 5.3 A negative feedback of $\beta = 0.002$ is applied to an amplifier of gain of 1000. Calculate the change in overall gain of the feedback amplifier if the internal amplifier is subjected to a gain reduction of 15%.

Hints: $A_f = \frac{A}{1+\beta A}$, $A' = (1-0.15)A$, $A_f' = \frac{A'}{1+\beta A'}$, $\frac{A_f - A_f'}{A_f} = ?$

Example 5.4.

The open loop gain of an amplifier changes by 20% due to change in internal prameters of basic amplifier. If 2% change in gain is allowed which type of feedback has to be applied? If the amplifier gain with feedback is 10, find the minimum value of the feedback ratio & the open-loop gain.

Hints: $\frac{dA_f}{A_f} = \frac{1}{1+A\beta} \cdot \frac{dA}{A}$

$\frac{dA}{A} = 20\%$ & $\frac{dA_f}{A_f} = 2\%$

Example 5.5. A feedback amplifier uses voltage sampling & series mixing topology. Input & output Impedance with out feedback 10kΩ & 100Ω respectively, Gain of the Basic amplifier is 100. Amount of feedback (negative) $\beta = 0.002$. Bandwidth without feedback is 100kHz. Determine with feed back (i) Input & output Impedance
(ii) Gain with feedback
(iii) Bandwidth with feedback

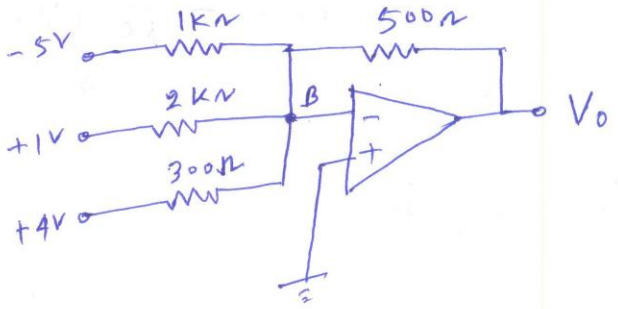
Hints: Identify topology & types of feedback & use required formula.

Example : 5.6 For an non-inverting amplifier using op-amp $R_f = 2k\Omega$, $R_i = 2k\Omega$, determine gain.

Hints:

$$A_f = 1 + \frac{R_f}{R_i}$$

Example : 5.7 Determine V_o of the circuit.



Hints Use nodal Analysis at point B & $V_B = 0V$.

Example 5.8 Sketch the circuit to get out $V_o = -V_1 + 2V_2 - 3V_3$, V_1, V_2 & V_3 are input voltages.

Hints Follow Summing Amplifier.

Take proper ratio of resistance corresponds to feedback & input.

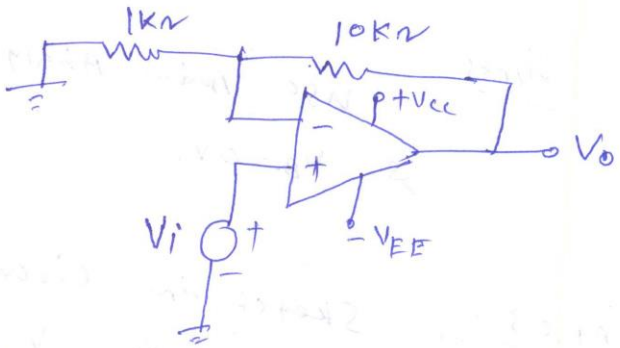
Example 5.9

A 10 mV, 2 kHz sinusoidal signal is applied to the inverting input terminal of an op-amp integrator for which R = 50kΩ & C = 2 μF. Determine output voltage.

Hints:

$$V_o = -\frac{1}{RC}\int_0^t V_{in}\,dt$$

Example 5-10



(a) For the circuit shown in fig. V_i = 15 mV, power supply voltage is ±15V. Determine V_o. If V_i is change to 2 volt, what is the value of V_o? Justify your answer.

(b) Repeat problem (a) if op-amp is desired with power supply voltage of ±30V.

Hints: Try to solve using $V_o = \left(1 + \frac{R_f}{R_i}\right) v_i$ & voltage transfer characteristics of op-amp.

3.8 Sample Questions

1. Choose correct Alternatives

i) If the differential and common mode gain of an op-amp are 50 and 0.2 respectively , the CMRR will be

a) 10 b) 250 c) 50.2 d) 49.8

ii) The open loop gain of an op-amp is 10^5 . An input signal of 1mv is applied at inverting terminal with the non-inverting terminal connected to ground . Supply voltage is ±15V . Consider there is no feed back. The output of the amplifier is close to

a) +100 V b) -100V c) +15 V d) -15 V

iii) Due to negative feedback overall voltage gain of an amplifier

a) increases b) decreases

c) remains intact d) always increases then saturated to 100

iv) An ideal operational amplifier is a

a) voltage control current source b) voltage controlled voltage source

c) current controlled voltage source d) current controlled current source

v) The open loop gain of an op-amp is 10^5 . An input signal of 1mv is applied at inverting terminal with the non-inverting terminal connected to ground . Supply voltage is ±10V . Consider there is no feed back. The output of the amplifier is close to

a) +100 V b) -100V c) +10 V d) -10 V

vi) Due to negative feedback noise in an amplifier

a) increases b) decreases

c) remains intact d) always increases then saturated to 40dB

2. Draw the circuit diagram of an adder using op-amp in non-inverting mode and explain its working.

3. Draw the voltage transfer characteristics of a non-ideal op-amp . List the characteristics of an ideal op-amp

4. a) With diagram explain different feedback topologies.

b) Derive an expression for overall gain with feedback in an amplifier.

c) For a feedback amplifier input resistance, output resistance and voltage gain without feedback are respectively 1 KΩ, 500 Ω and 100. If negative feedback is provided to the amplifier with feedback ratio (β) of 4%, determine input resistance, output resistance and overall gain of the amplifier with feedback. Consider amplifier has been configured using voltage sampling and series mixing topology.

5. Mention the advantages of negative feedback in amplifier. Draw the block diagram of series – series topology in a feedback amplifier

6. Explain the following for an op-amp.

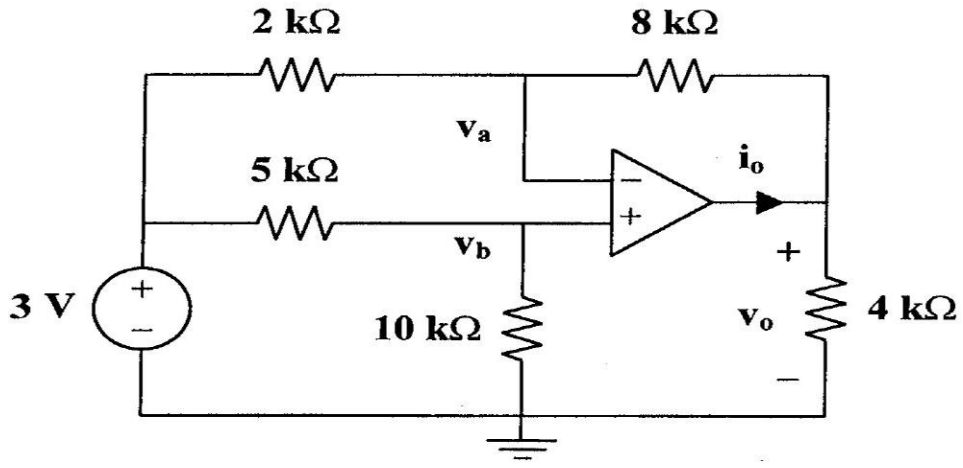
a) slew rate b) input bias current c) off-set null

7. a) Draw the circuit diagram of a basic differentiator using op-amp . Find an expression for output voltage from the differentiator.

b) Draw the output waveform from a differentiator with following input

(i) Sine wave (ii) Square wave

iii) Determine V_O and i_O in the following circuit . Consider op-amp is ideal one and operating at power supply voltage of ±15 V .



8. Derive an expression for input impedance with feedback in an amplifier configured with series sampling and shunt mixing topology .

9. Describe the op-amp as (i) an inverting amplifier (ii) a non-inverting amplifier

10. a) What is regenerative and degenerative feedback ?

b) What are the effects of feedback in an amplifier?

c) The open loop gain of an amplifier changes by 20 % due to changes in parameters of the active amplifying device. If a change of gain by 2 % is allowable, what type of feedback has to be applied ? If the amplifier gain with feedback is 10, find the minimum value of the feedback ratio and the open loop gain .

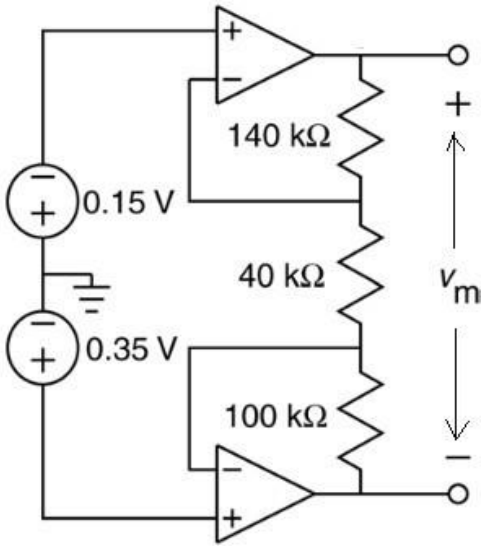
11. a) State Barkhausen criterion for oscillation.

b) What are the characteristics of an ideal op-amp?

c) What is virtual ground and virtual short?

12. a) Describe the application of op-amp as a voltage follower.

b) For the circuit shown in figure find out the voltage V_m. Consider op-amps are ideal and operating at power supply voltage of ± 15 V .



13. Write down the short notes of the followings

(a) Barkhausen Criterion
(b) Op-Amp Integrator
(c) Feedback topology
(d) Bandwidth with feedback
(e) Practical differentiator
(f) Practical Integrator

Assignments

1. How bandwidth of an amplifier changes with respect to feedback
2. How stability of gain is improved using negative feedback?
3. Compare among different feedback topologies considering parameters input impedance, output impedance, bandwidth, non-linear distortion
4. Derive an expression for close loop gain of a non- inverting amplifier using one op-amp having finite open loop gain of A.
5. Derive an expression for output voltage of op-amp based integrator.

MODULE IV

DIGITAL ELECTRONIC PRINCIPLES:

We know there are two types of signals, one is analog or continuous signal and the second one is Digital or discrete signal. So the science or field of research in the area of engineering is termed as Analog and **Digital Electronics** respectively. Now coming to the area of Digital Electronics, it is essential to understand wide range of applications from industrial electronics to the fields of communication, from micro embedded systems to military equipment. The main and perhaps the most revolutionary **advantage of digital electronics** is the decrease in size and the improvement in technology.

Advantages of digital signal

- Carry more information per second than analogue signals
- Maintain quality over long distances better than analogue signals.
- They're automatic
- Easier to remove noise
- Can be very immune to noise

Binary Digit and Logic Levels

There are two digits in binary system. 0 and 1 called bits. Bit is contraction of two words **Bi**nary Digi**t**.

Digital Waveforms

Digital waveform are voltages levels changing back and forth between HIGH and LOW levels or states.Usually these waveforms are represented as timing diagrams used to represent wave behavior relative to time,

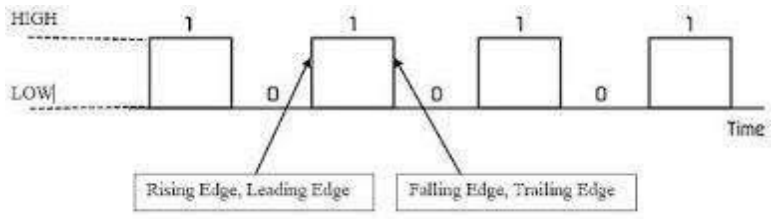


Figure 2

Pulse indicated in Figure 2 has two edges: A leading edge where pulse goes to HIGH from LOW state and Falling edge where pulse revert. However it is non ideal pulse representation because sudden transition from one state to other is impractical. Depending on practical consideration it will take small amount of time to get HIGH transition from LOW and vice versa,

Rise Time: ***Time required for pulse to go from its LOW level to HIGH is called rise time*** **tr.**

Fall Time: ***Time required for pulse to go from its HIGH level to LOW level is called fall time*** **tf.**

Pulse Width: ***It is measure of duration between rise edge and fall edge of the pulse indicated as*** **tw.**

Frequency (*f*) *and Time Period T:*

Frequency of a periodic (which repeats itself) waveform is the rate at which it repeats itself and measured in *Hz*. Whereas time period is duration after that signal or waveform repeats itself. Mathematical interpretations are given below in equation *(i)* and *(ii)* .

$$f = 1/T \ \ \textbf{Hz} \qquad (i)$$

$$T = 1/f \ \ \textbf{s} \qquad (ii)$$

Duty Cycles

A more essential characteristic of a periodic signal that is ratio of pulse width to the time period.

Duty Cycle = *(Pulse-width / T) 100%*

1. Decimal Number System

The number system that we use in our day-to-day life is the decimal number system. Decimal number system has base 10 as it uses 10 digits from 0 to 9. In decimal number system, the successive positions to the left of the decimal point represents units, tens, hundreds, thousands and so on.

Each position represents a specific power of the base (10). For example, the decimal number 1234 consists of the digit 4 in the units position, 3 in the tens position, 2 in the hundreds position, and 1 in the thousands position, and its value can be written as

2.	**Binary Number System** Base 2. Digits used: 0, 1
3	**Octal Number System** Base 8. Digits used: 0 to 7
4	**Hexa Decimal Number System** Base 16. Digits used: 0 to 9, Letters used: A- F

Binary to Decimal Conversion

Conversion of Integer Numbers

Just as you can convert any binary numbers to hexadecimal, or convert binary numbers to octal, any number in the binary number system can be converted into the hexadecimal number system. This conversion is also very simple method. Let, a binary number be $(11010)_2$, where the weight of the binary digits from most significant bit are 2^4, 2^3, 2^2, 2^1, 2^0 respectively.

Now the bits are multiplied with their weights, and the sum of those products is the respective decimal number. Now let us follow the following steps mathematically:

$$(11010)_2 \rightarrow 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$$
$$= 16 + 8 + 2 = (26)_{10}$$
$$\therefore (11010)_2 = (26)_{10}$$

Hence, $(26)_{10}$ is the required decimal number. This is how binary to decimal conversion is performed. As another example, we convert the binary number $(1110)_2$ to a decimal number:

$$(1110)_2 = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = (15)_{10}$$

Convert Binary Number to Decimal Number

Conversion of Decimal Point Number to Decimal

This can also be done in the same way, however after the decimal point the number should be multiplied with 2^{-1}, 2^{-2} etc.
For example,

$$(1110.011)_2 = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 + 0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3}$$
$$= (15.375)_{10}$$

Decimal to Binary Conversion

Integer Decimal Numbers to Binary

Divide the number by 2 and take only the remainder, if division is completed than take only the remainder which gives the binary number. Suppose we are converting the decimal number $(87)^{10}$. We divide 87 by 2 and get 43 as the quotient and 1 as the remainder. These remainders are written beside as shown below.

2	87	→ 1
2	43	→ 1
2	21	→ 1
2	10	→ 0
2	5	→ 1
2	2	→ 0
	1	

The possibility of remainder $(87)_{10} = (1010111)_2$ is only 1 and 0. Thus the number is counted from the last remainder. Such as 1 → 0 → 1 → 0 → 1 → 1 → 1. This is how **decimal to binary conversion** is done.

Fraction Decimal Numbers to Binary

In this case, the successive multiplication is done. The number which is to be converted is multiplied with base or radix of binary number which is 2. The integer part or the carry of the product is taken out and the same process is repeated until we get an integer. For example-The binary equivalent of $(.95)_{10}$ is evaluated as follows-

$$.95 \times 2 = 1.90 - - - - - - - - - - 1 \; is\ taken\ out$$
$$.90 \times 2 = 1.80 - - - - - - - - - - 1$$
$$.80 \times 2 = 1.60 - - - - - - - - - - 1$$
$$.60 \times 2 = 1.20 - - - - - - - - - - 1$$
$$.20 \times 2 = .40 - - - - - - - - - - - - 1$$
$$.40 \times 2 = .80 - - - - - - - - - - - - 0$$

Since, we are not getting the integer value after successive multiplication, we can approximate the value to be $(.111110\ldots.)_2$.

Negative Decimal to Binary

In case of a negative number we can go for 2's complement representation of a signed number. Example- 9 = 0000 1001
1's complement = 1111 0110.
Adding 1 we get = 11110111 which is the 2's complement representation of (-9).

Binary representation of 5 is: 0 1 0 1

1's Complement of 5 is: 1 0 1 0

2's Complement of 5 is: (1's Complement + 1) i.e.

1 0 1 0 (1's Compliment)

\+ 1

1 0 1 1 (2's Complement i.e. -5)

BINARY ARITHMETIC

The **arithmetic of binary numbers** means the operation of addition, subtraction, multiplication and division. **Binary arithmetic** operation starts from the least significant bit i.e. from the right most side. Binary Addition

There are four steps in binary addition, they are written below

- 0 + 0 = 0
- 0 + 1 = 1
- 1 + 0 = 1
- 1 + 1 = 0 (carry 1 to the next significant bit)

An example will help us to understand the addition process. Let us take two binary numbers 10001001 and 10010101

```
    1
 10001001
 10010101
---------
100111110
```

The above example of **binary arithmetic** clearly explains the binary addition operation, the carried 1 is shown on the upper side of the operands.

Binary Subtraction

Here are too four simple steps to keep in memory

- 0 – 0 = 0
- 0 – 1 = 1, borrow 1 from the next more significant bit
- 1 – 0 = 1
- 1 – 1 = 0

Suppose, A = 10101100 and B = 1010100 and we want to find out
A – B. Now implementing the rules of binary subtraction

```
1 0 1 0 1 1 0 0
  1 0 1 0 1 0 0
-----------------
              0
```

The first step is 0 – 0 = 0 and that's what is written in the place for result

```
1 0 1 0 1 1 0 0
  1 0 1 0 1 0 0
-----------------
            0 0
```

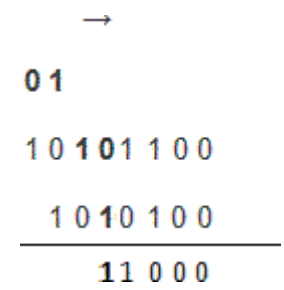
Similarly again the last step is repeated as here the numbers are both 0 and from the table we know 0 – 0 = 0.

```
1 0 1 0 1 1 0 0
  1 0 1 0 1 0 0
-----------------
          0 0 0
```

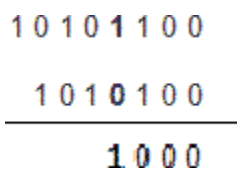
From the table we can find out that 1 – 1 = 0 and it is written

```
1 0 1 0 1 1 0 0
  1 0 1 0 1 0 0
-----------------
        1 0 0 0
```

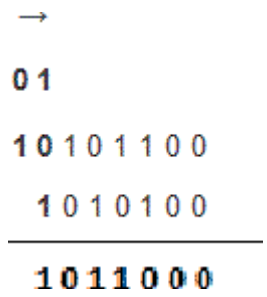
The table shows that 1 – 0 = 1 and we have written exactly that in result



Here 0 – 1 = 1 with borrowing of 1 from the next significant bit and that's what has been done. We will treat the next 1 as 0 in the next step as shown below.



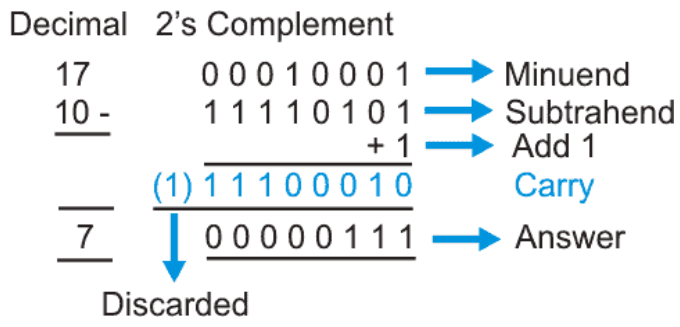
As the 1 was borrowed in the previous step we are treating the 1 as 0 and the result is 0 – 0 = 0 and that is written



Again the last 1 has been borrowed because the operation done was 0 – 1 = 1 with borrow 1 from the next most significant bit and the final result of **binary subtraction**, we got is written in the place of result in the final step. Why We Do Need 2's Complement?

The main problem of using **2's complement** is that it can be used for subtraction for two binary digits. The computer understands only binary as we know, and there is nothing called as negative number in the binary number system but it is absolutely necessary to represent a negative number using binary which can be done by assigning a sign bit to the number which is an extra bit required. If the sign bit is 1 then number is considered negative and if it is 0, than it will be the number will be called as positive.
For subtraction of binary numbers that can be done as follows-
Subtracting a Smaller Number from a Larger Number

1. **Find 2's complement of the smaller number.**
2. **Add the larger and 2's complement of the smaller number.**
3. **Discard the carry.**
4. **After discarding the carry, keep the result which will be answer for subtraction.**



Subtracting Larger Number from Smaller Number

1. Find 2's complement of larger number.
2. Add 2's complement of larger number to the smaller number.
3. If no carry is generated, find the 2's complement of the result and the result will be negative.
4. If carry is generated, discard the carry and take the result which will be the answer and the sign will be negative.

+ 75 0 1 0 0 1 0 1 1
- 75 1 0 1 1 0 1 0 1 (2's Complement form)

+ 26 0 0 0 1 1 0 1 0
- 75 1 0 1 1 0 1 0 1 (2's Complement form of - 75)
- 49 1 1 0 0 1 1 1 1 (No Carry)

Subtraction of larger number from smaller number.

Binary Multiplication

Like in case of binary addition and **binary multiplication** there are also four steps to be followed during a bigger multiplication or we can say these fundamental steps as well.
These are

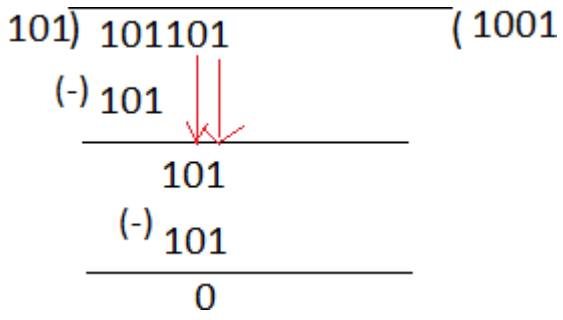
$0 \times 0 = 0$
$1 \times 0 = 0$
$0 \times 1 = 0$
$1 \times 1 = 1 (there\ is\ no\ carry\ or\ borrow\ for\ this)$

```
   1011.01
 ×   110.1
 -------
   101101
  0000000
 10110100
1011010000
-----------
1001001.001
```

Binary Division

Binary division is an important but often overlooked part of binary arithmetic. Though it is not too difficult, it may look a bit tougher than the other binary operations because all the other had some similarity among

themselves like they all had four basic steps which made all the processes quite easy to understand. But the process of binary **division** does not have any ***specific*** rules to follow.



LOGIC GATES AND BOOLEAN ALGEBRA

Boolean algebra or switching algebra is a system of mathematical logic to perform different mathematical operations in binary system. These are only two elements 1 and 0 by which all the mathematical operations are to be performed. There only three basis binary operations, AND, OR and NOT by which all simple as well as complex binary mathematical operations are to be done. There are many rules in Boolean algebra by whichthose mathematical operations are done. In Boolean algebra, the variables are represented by English Capital Letter like A, B, C etc and the value of each variable can be either 1 or 0, nothing else.

Some basic logical Boolean operations- AND operation,

$$0.0 = 0$$
$$0.1 = 0$$
$$1.0 = 0$$
$$1.1 = 1$$

OR operation,

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 1$$

Not operation,

$$\overline{1} = 0$$
$$\overline{0} = 1$$

Some basic laws for Boolean Algebra,

$$\overline{0} = 1, \overline{1} = 0, \; if \; A = 1 \; then \; \overline{A} = 0 \; and \; if \; A = 0, \; then \; \overline{A} = 1.$$

A . 0 = 0 where A can be either 0 or 1.
A . 1 = A where A can be either 0 or 1.
A . A = A where A can be either 0 or 1.
A . $\bar{A}$ = 0 where A can be either 0 or 1. A + 0 = A where A can be either 0 or 1. A + 1 = 1 where A can be either 0 or 1. A + $\bar{A}$ = 1
A + A = A
A + B = B + A where A and B can be either 0 or 1.

A . B = B . A where A and B can be either 0 or 1.
The laws of Boolean algebra are also true for more than two variables like, Cumulative Laws for Boolean Algebra

$$A+B+C=A+C+B=B+A+C=B+C+A=C+A+B=C+B+A$$
$$A.B.C=A.C.B=B.A.C=B.C.A=C.A.B=C.B.A$$

Associative Laws for Boolean Algebra

$$(A+B)+C=A+(B+C)$$
$$(A.B).C=A.(B.C)$$

Distributive Laws for Boolean Algebra

$$A.(B+C)=A.B+A.C$$

Redundant Literal Rule

$$AA+\overline{A}A+AB+\overline{A}B$$

Rules of Boolean Algebra

$1.A+0=A$	$7.A\bullet A=A$
$2.A+1=1$	$8.A\bullet\overline{A}=0$
$3.A\bullet 0=0$	$9.\overline{\overline{A}}=A$
$4.A\bullet 1=A$	$10.A+AB=A$
$5.A+A=A$	$11.A+\overline{A}B=A+B$
$6.A+\overline{A}=1$	$12.(A+B)(A+C)=A+BC$

A, B, and C can represent a single variable or a combination of variables.

DE MORGAN'S THEREM,

$$\overline{A+B}=\overline{A}\,\overline{B}$$
$$and\ \ \overline{AB}=\overline{A}+\overline{B}$$

Proof from truth table,

Inputs		Outputs			
A	B	$\overline{A+B}$	$\overline{A}.\overline{B}$	$\overline{AB}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	0	0	1	1
1	0	0	0	1	1
1	1	0	0	0	0

$$Column\ for\ \overline{A+B}\ and\ \overline{A}.\overline{B}\ are\ same.$$

$$Column\ for\ \overline{AB}\ and\ \overline{A}+\overline{B}\ are\ same.$$

Examples of Boolean Algebra

$$Simplify,\ \overline{(A+\overline{B})(C+\overline{D})}$$

$$Here,\ \overline{(A+\overline{B})(C+\overline{D})}\ [\ As\ per\ De\ Morgan\ Therem\ \overline{x.y}=\overline{x}+\overline{y}\ ]$$

$$=\overline{(A+\overline{B})(C+\overline{D})}\ [\ As\ per\ De\ Morgan\ Therem\ \overline{x+y}=\overline{x}.\overline{y}\ ]$$

$$=\overline{A}.\overline{\overline{B}}+\overline{C}.\overline{\overline{D}}$$

$$=\overline{A}B+\overline{C}D$$

These are another method of simplifying complex Boolean expression. In this method we only use three simple steps.

1. Complement entire Boolean expression.
2. Change all ORs to ANDs and all ANDs to ORs.
3. Now, complement each of the variable and get final expression.

By this method,

$\overline{(A+\overline{B})(C+\overline{D})}$ will be first complemented, i.e. $(A+\overline{B})(C+\overline{D})$ .Now, change all (+) to (.) and (.) to (+) i.e.$A\overline{B}+C\overline{D}$. Now, complement each of the variable,$\overline{A}B+\overline{C}D$.

This is the final simplified form of Boolean expression, $\overline{(A+\overline{B})(C+\overline{D})}$
And it is exactly equal to the results which have been come by applying De Morgan Theorem.
Another example,

$$\overline{\overline{AB}+\overline{A}+AB}=\overline{\overline{AB}}.\overline{\overline{A}}.\overline{AB}\quad[Appling\ De\ Morgan\ Therem]$$

$$=AB.A.\overline{AB}$$

$$=AB.\overline{AB}.A=0$$

By Second Method,

$$\overline{\overline{AB}+\overline{A}+AB}=\overline{\overline{A+B}.\overline{A}.A+B}=(\overline{\overline{A}+\overline{B}}).A.(\overline{A}+\overline{B})=0$$

$$Example\ simplify,\ AB+A\overline{B}C+B\overline{C}=A(B+\overline{B}C)+B\overline{C}=A(B+\overline{B})(B+C)+B\overline{C}$$

$$=AB+AC+B\overline{C}=AB(C+\overline{C})+AC+B\overline{C}=ABC+AB\overline{C}+AC+B\overline{C}$$

$$=AC(1+B)+B\overline{C}(A+1)=AC+B\overline{C}$$

Representation of Boolean function in truth

$$f(A,B,C) = \overline{A}B + \overline{B}C.$$

table. Let us consider a Boolean function,

Now let us represent the function in truth table.

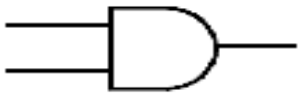
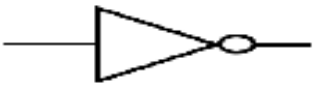
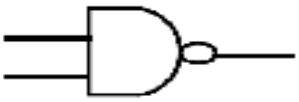
A	B	C	$\bar{A}B$	$\bar{B}C$	$\bar{A}B+\bar{B}C$
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	0	0	0
1	1	1	0	0	0

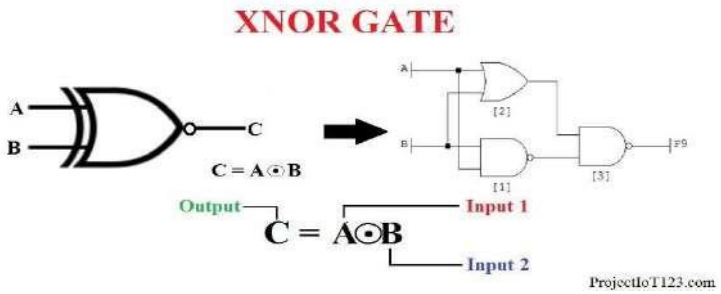
LOGIC GATES:

Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship between the input and the output is based on a **certain logic**. Based on this, logic gates are named as AND gate, OR gate, NOT gate etc. Logic gates are primarily implemented using diodes or transistors acting as electronic switches. **Logic circuits** include such devices as multiplexers, registers, arithmetic logic units (ALUs), and computer memory, all the way up through complete microprocessors, which may contain more than 100 million gates. In modern practice, most gates are made from MOSFETs (metal–oxide–semiconductor field-effect transistors).

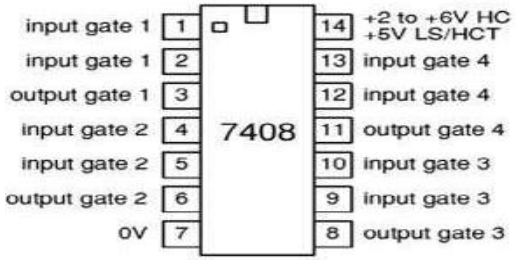
Compound logic gates AND-OR-Invert (AOI) and OR-AND-Invert (OAI) are often employed in circuit design because their construction using MOSFETs is simpler and more efficient than the sum of the individual gates.

LOGIC GATES AND THEIR TRUTH TABLES:

Gate Name	Symbol	Notation	Truth table
AND		F = A.B or F= AB	A B A.B 0 0 0 0 1 0 1 0 0 1 1 1
OR		F = A+B	A B A+B 0 0 0 0 1 1 1 0 1 1 1 1
NOT		F=A or F = A′	A F 0 1 1 0
NAND		F = (A . B)	A B F 0 0 1 0 1 1 1 0 1 1 1 0
NOR		F = (A + B)	A B F 0 0 1 0 1 0 1 0 0 1 1 0
XOR		F = A⊕B F = A′B + AB′	A B F 0 0 0 0 1 1 1 0 1 1 1 0



AND GATE IC (2 INPUT):EXAMPLE OF LOGIC GATE



BOOLEAN FUNCTION

The use of switching devices like transistors give rise to a special case of the Boolean algebra called as switching algebra. In switching algebra, all the variables assume one of the two values which are 0 and 1.In Boolean algebra, 0 is used to represent the 'open' state or 'false' state of logic gate. Similarly, 1 is used to represent the 'closed' state or 'true' state of logic gate. A Boolean expression is an expression which consists of variables, constants (0- false and 1-true) and logical operators which results in true or false. A Boolean function is an algebraic form of Boolean expression. A Boolean function of n-variables is represented by f(x1, x2, x3….xn). By using Boolean laws and theorems, we can simplify the Boolean functions of digital circuits. A brief note of different ways of representing a Boolean function is shown below.

- Sum-of-Products (SOP) Form
- Product-of-sums (POS) form
- Canonical forms

DOMAIN OF EXPRESSION:It is the set of variables present in that expression.

Sum of Product (SOP) Form

The sum-of-products (SOP) form is a method (or form) of simplifying the Boolean expressions of logic gates. In this SOP form of Boolean function representation, the variables are operated by AND (product) to form a product term and all these product terms are ORed (summed or added) together to get the final function. A sum-of-products form can be formed by adding (or summing) two or more product terms using a Boolean addition operation. Here the product terms are defined by using the AND operation and the sum term is defined by using OR operation. The sum-of-products form is also called as Disjunctive Normal Form as the product terms are ORed together and Disjunction operation is logical OR.

STANDARD SOP: A Standard SOP is the one in which all the variables in domain appear in each product term in expression. ex: A'BC + AB'C + ABC ' + ABC

Non-standard SOP: AB + ABC + CDE

SOP form representation is most suitable to use them in FPGA (Field Programmable Gate Arrays).

Examples

AB + ABC + CDE

A'BC + AB'C + ABC' + ABC

SOP form can be obtained by

- Writing an AND term for each input combination, which produces HIGH output.
- Writing the input variables if the value is 1, and write the complement of the variable if its value is 0.
- OR the AND terms to obtain the output function.

Product of Sums (POS) Form

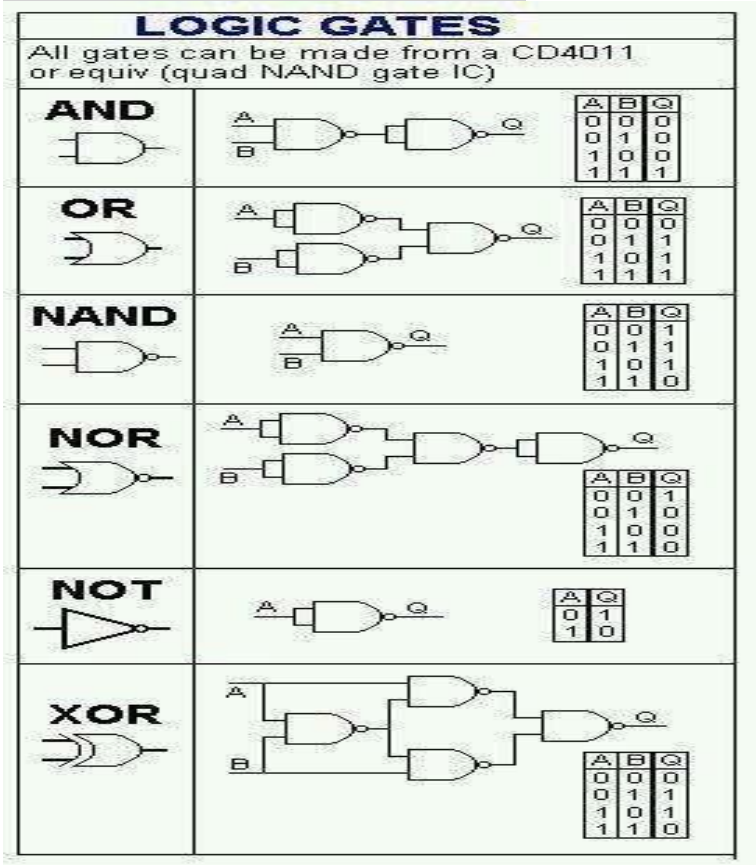
The product of sums form is a method (or form) of simplifying the Boolean expressions of logic gates. In this POS form, all the variables are ORed, i.e. written as sums to form sum terms. All these sum terms are ANDed (multiplied) together to get the product-of-sum form. This form is exactly opposite to the SOP form. So this can also be said as "Dual of SOP form". Here the sum terms are defined by using the OR operation and the product term is defined by using AND operation. When two or more sum terms are multiplied by a Boolean OR operation, the resultant output expression will be in the form of product-of-sums form or POS form. The product-of-sums form is also called as Conjunctive Normal Form as the sum terms are ANDed together and Conjunction operation is logical AND. Product-of-sums form is also called as Standard POS.

Examples :(A+B) (A + B + C) (C +D)**(NON Standard POS)**

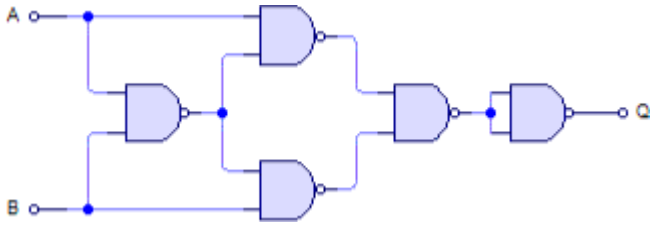
(A + B + C) (A + B + C ') (A + B' + C) (A' + B + C)**(Standard POS)**

UNIVERSAL GATES-NAND AND NOR GATES:

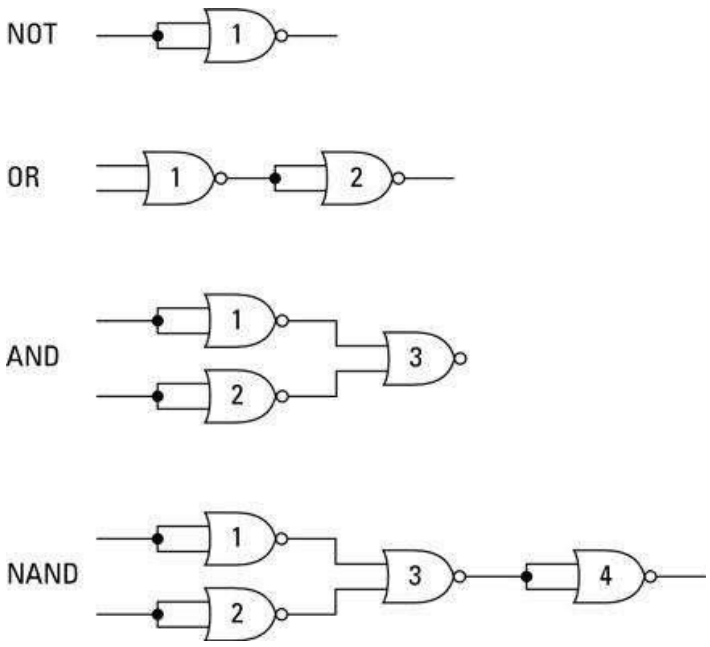
NAND GATE AS UNIVERSAL GATE:



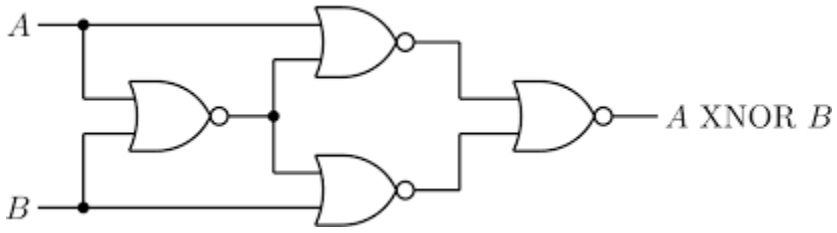
EX-NOR GATE FROM NAND GATE



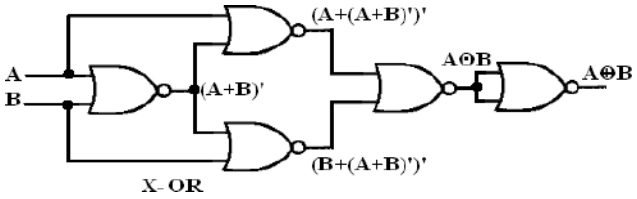
NOR GATE AS UNIVERSAL GATE:



EXNOR GATE FROM NOR GATE



EXOR GATE FROM NOR GATE



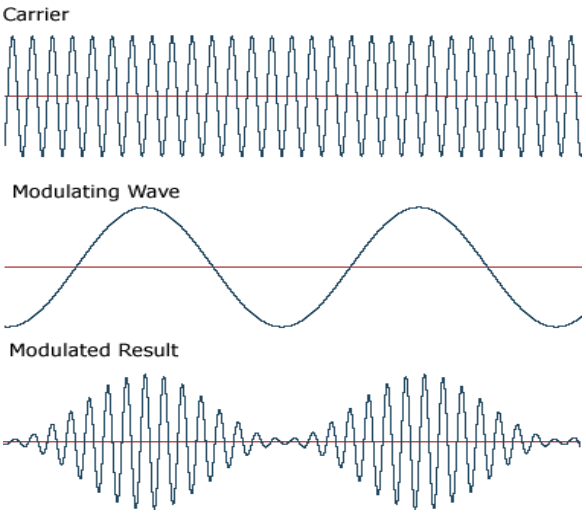
Module-V: Communication System, Satellite and Radar System and Wireless communication (8L)

Principles of Communication:

Modulation is the process by which some characteristics of a high frequency wave called the carrier, is changed according to the instantaneous value of a low frequency wave called the modulating wave. The resultant wave is called the modulated wave.

Amplitude Modulation:

Amplitude modulation is obtained by varying the amplitude of the carrier by the modulating signal, the change in amplitude from the unmodulated value being proportional to the instantaneous value of the modulating signal independent of its frequency.



Modulating signal in sinusoidal form can be written as

$v_m = V_m \cos w_m t$

Carrier wave can be written as

$v_c = V_c \cos w_c t$

The amplitude of the modulated carrier is

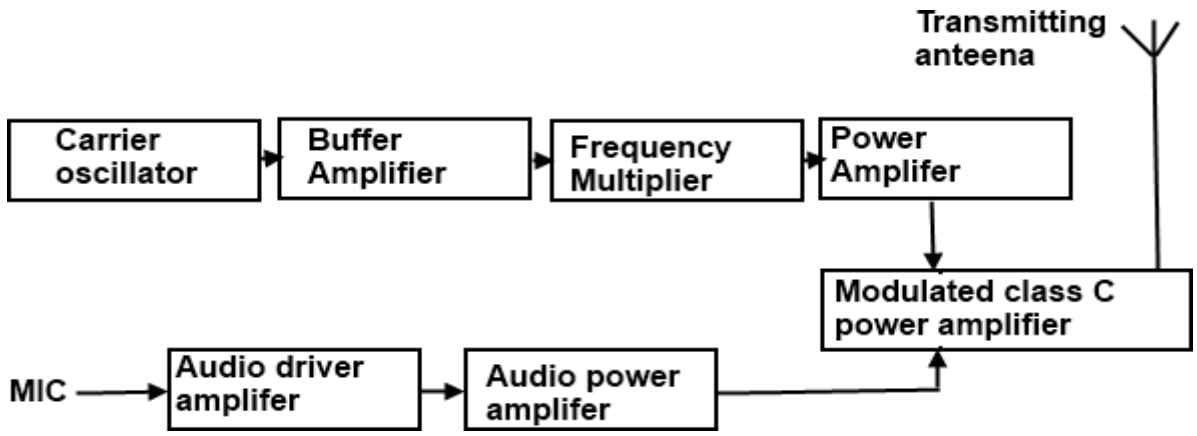
$V(t) = V_c + K_a V_m \cos w_m t$ where K_a is the proportionality constant.

The amplitude modulated carrier is represented by

$(v_c)_{AM} = V_c(1+m\cos w_m t)\cos w_c t$

where m(=K_aV_m/V_c) is known as the modulation index.

AM Transmitter:



CARRIER OSCILLATOR

A oscillator is used to operate the transmitted at a desirable fixed radio frequency (RF).The power output of the oscillator,being not sufficiently large,is amplified in several stage to the desirable.

BUFFER AMPLIFIER

This amplifier isolates the oscillate from the succeeding stage, so that the variation of coupling and antenna loading do not influence the oscillator frequency.

FREQUENCY MULTIPLIER

Oscillator cannot generate very high carrier frequencies. To obtain such frequencies, the frequency multiplier is used to multiply the frequency of oscillator output signal to the required value.

POWER AMPLIFIER

The modulated carrier is fed to this stage for final amplification before being carried to the antenna.

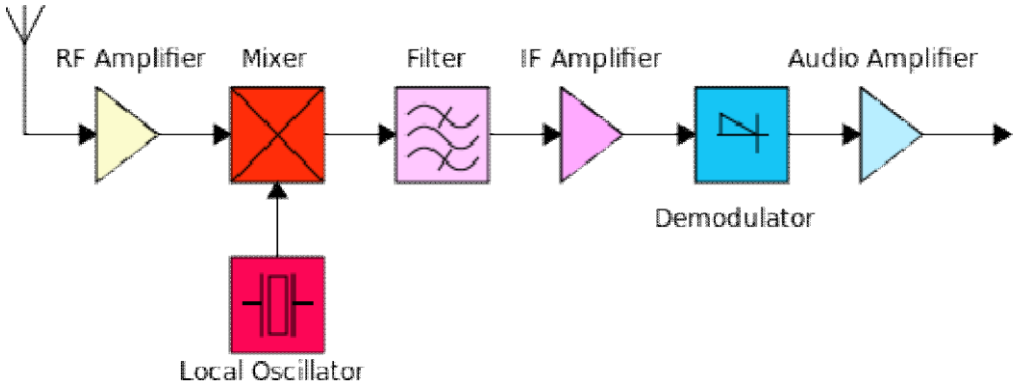
AUDIO AMPLIFIER

This amplifier is used to amplify the audio signal output of the microphone that converts the speech or music to be transmitted into equivalent electrical signal.

MODULATOR

The function of the modulator is to amplitude modulate the RF carriernin accordance with the amplified audio signal.

AM RECIEVER



ANTENNA

The antenna picks up all radiated signals and feeds them into the RF amplifier. These signals are very small (usually only a few microvolt).

RF AMPLIFIER

This circuit can be adjusted (tuned) to select and amplify any carrier frequency within the AM broadcast band. Only the selected frequency and its two side bands pass through the amplifier. (Some AM receivers don't have a separate RF amplifier stage.)

LOCAL OSCILLATOR

This circuit generates a steady sine wave at a frequency 455 KHz above the selected RF frequency.

MIXER

This circuit accepts two inputs, the amplitude modulated RF signal from the output of the RF amplifier (or the antenna when there is no RF amplifier) and the sinusoidal output of the local oscillator (LO). These two signals are then "mixed" by a nonlinear process called *heterodyning* to produce sum and difference

frequencies. For example, if the RF carrier has a frequency of 1000 KHz, the LO frequency is 1455 KHz and the sum and difference frequencies out of the mixer are 2455 KHz and 455 KHz, respectively. The difference frequency is always 455 KHz no matter what the RF carrier frequency.

IFAMPLIFIER

The input to the If amplifier is the 455 KHz AM signal, a replica of the original AM carrier signal except that the frequency has been lowered to 455 KHz, The IF amplifier significantly increases the level of this signal.

DETECTOR

This circuit recovers the modulating signal (audio signal) from the 455 KHz IF. At this point the IF is no longer needed, so the output of the detector consists of only the audio signal.

AUDIOANDPOWERAMPLIFIERS

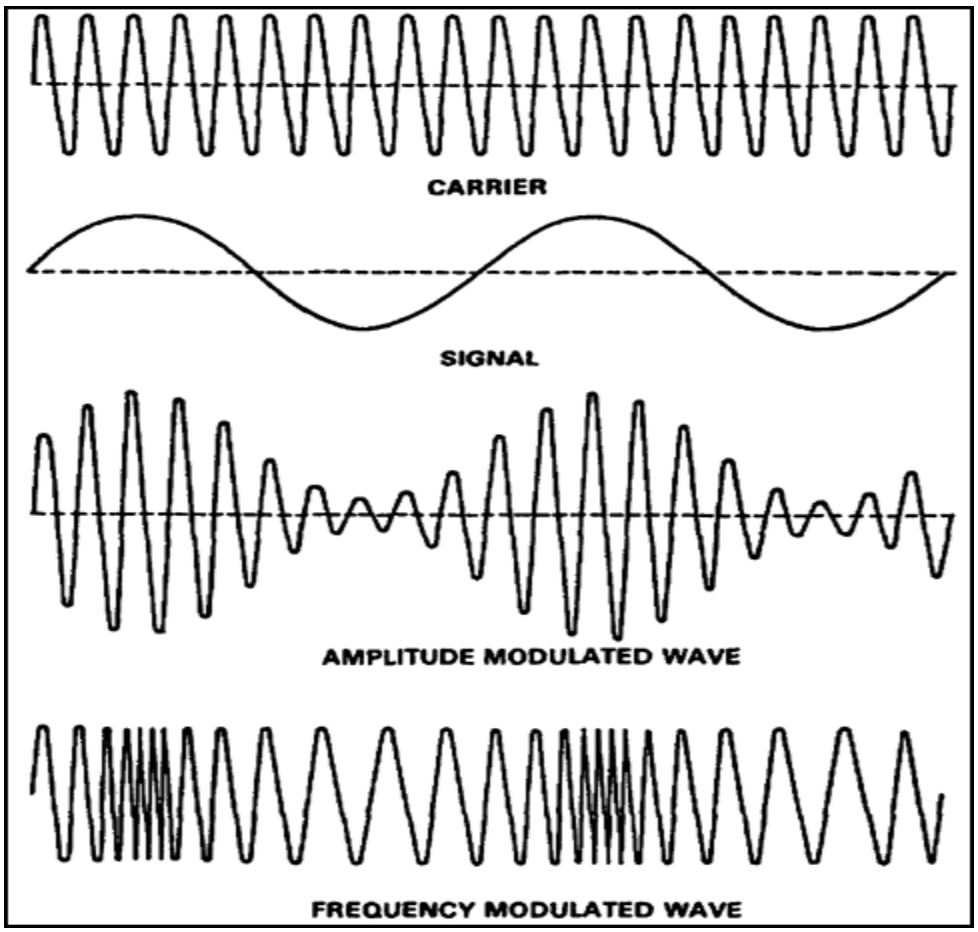
This circuit amplifies the detected audio signal and drives the speaker to produce sound.

FM MODULATION

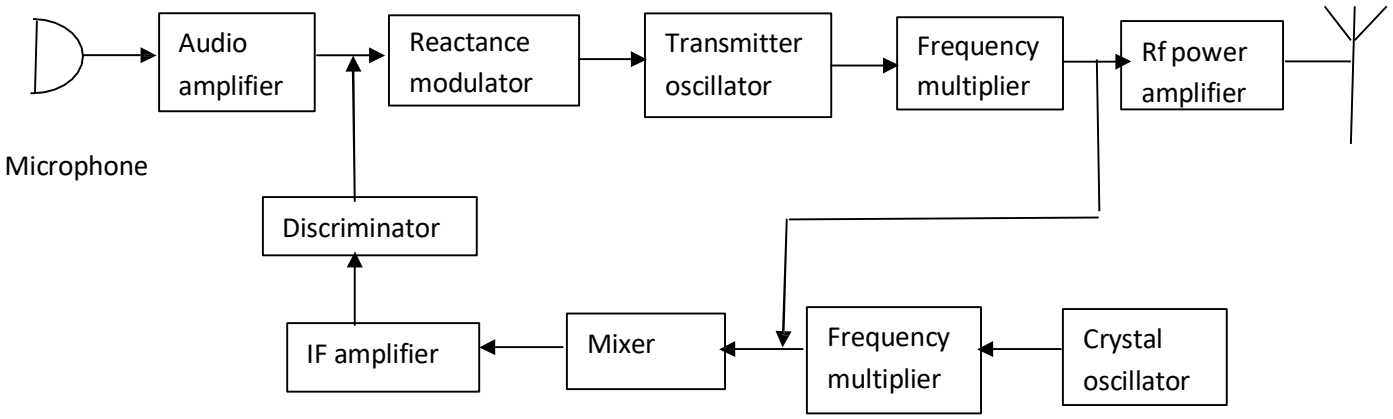
Mathematically, a frequency modulated (FM) waveform can be described using the equation

$$s(t) = A_c \cos\left[2\pi f_c t + 2\pi k_f \int_0^t m(\tau)\, d\tau\right]$$

where s(t) is the FM wave, Accos2πfct is the high frequency sinusoidal carrier and m(t) is the baseband message signal (the voice signal). The parameter kf is the frequency sensitivity of the FM modulator.



FM TRANSMITTER



AUDIO AMPLIFIER

It amplifies the audio signal from the microphone which converts the sound into equivalent electrical signal.

REACTANCE MODULATOR

This transforms the audio amplitude changes into frequency changes of the transmitter oscillator.

TRANSMITTER OSCILLATOTR

An RF oscillator is used here to generate the desirable oscillations.

FREQUENCY MULTIPLIER

A number of frequency multipliers are used in this stage to raise the frequency to the required value.

MIXER

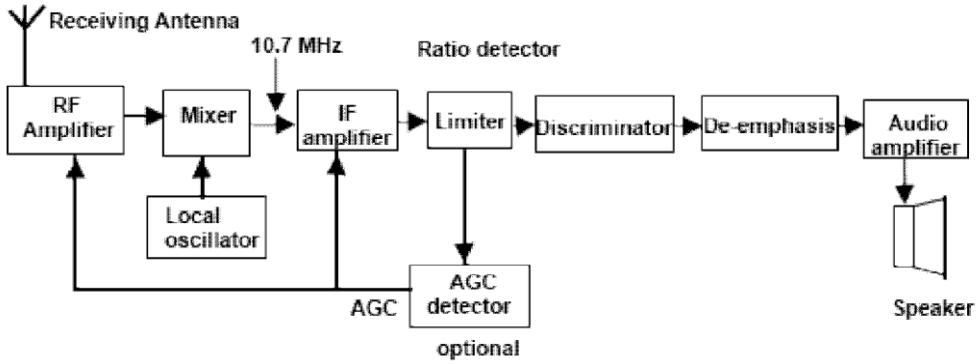
A part of the output of block of frequency f_c and that of frequency f_o .The frequency multipler block beat together in the mixer stage to produce a f_c-f_o Signal.

IF AMPLIFIER

The IF amplifier significantly increases amplitude of f_c-f_o frequency component signal.

DISCRIMINATOR: The output of the IF amplifietr is applied to a phase discriminator which gives a zero DC output voltage if the frequency of its input signal to which it is tuned remains constant.

FM RECEIVER



The RF amplifier amplifies the received signal intercepted by the antenna. The amplified signal is then applied to the mixer stage.

The second input of the mixer comes from the local oscillator. The two input frequencies of the mixer generate an IF signal of 10.7 MHz. This signal is then amplified by the IF amplifier..

The output of the IF amplifier is applied to the limiter circuit. The limiter removes the noise in the received signal and gives a constant amplitude signal. This circuit is required when a phase discriminator is used to demodulate an FM signal.

The output of the limiter is now applied to the FM discriminator, which recovers the modulating signal. However, this signal is still not the original modulating signal. Before applying it to the audio amplifier stages, it is de-emphasized.

De-emphasizing attenuates the higher frequencies to bring them back to their original amplitudes as these are boosted or emphasized before transmission. The output of the de-emphasized stage is the audio signal, which is then applied to the audio stages and finally to the speaker. It should be noted that a limiter circuit is required with the FM discriminators. If the demodulator stage uses a ratio detector instead of the discriminator, then a limiter is not required. This is because the ratio detector limits the amplitude of the received signal. In Figure (a) a dotted block that covers the limiter and the discriminator is marked as the ratio detector.

In FM receivers, generally, AGC is not required because the amplitude of the carrier is kept constant by the limiter circuit. Therefore, the input to the audio stages controls amplitudes and there are no erratic changes the volume level. However, AGC may be provided using an AGC detector. This generates a dc voltage to control the gains of the RF and IF amplifier.